

Overview

XJAnalyser is a visual analysis and debugging tool for devices in your JTAG chain. It provides instant chain verification as part of the simple 3-step set-up, and then gives you an interactive graphical view of the pins on your JTAG devices.

You can group pins into busses for easier control, and quickly generate toggling signals to trace connections around your board—useful when verifying shorts or opens. XJAnalyser also supports the STAPL/JAM and SVF standards for programming JTAG devices in-system.

Graphical circuit debugging

When tracing a net around your board with an oscilloscope, set a pin on the net to toggle and capture the signal at different points. If you slip to another pin, you will instantly know that you are no longer tracing the signal of interest.

Quickly locate signals you are sending to a device. By monitoring pins with changing values you can, for instance, press a button and quickly locate and display the pin/ball it is connected to, even if there are many thousands of pins/balls on the devices in your chain.

See the section of the chain of interest. For devices with large numbers of pins/balls, the information can become overwhelming. XJAnalyser solves this problem by enabling you to zoom in on just the balls or pins that you are interested in. You can also display multiple views of the JTAG chain, showing different areas of interest.

Flexible control

Control the devices in your JTAG chain the way you want to. XJAnalyser offers three methods for controlling pins: directly through the graphic display, or by using the pin list or pin watch. The pin watch also allows you to group pins into busses; you can then write a value to a complete bus all at once.

JTAG chain interaction

The intuitive graphical interface allows rapid interaction with the devices in the JTAG chain without programming or booting any devices on your board.

Monitor the states of all the I/O pins in real-time and graphically set pins to output high, low or toggle as required.

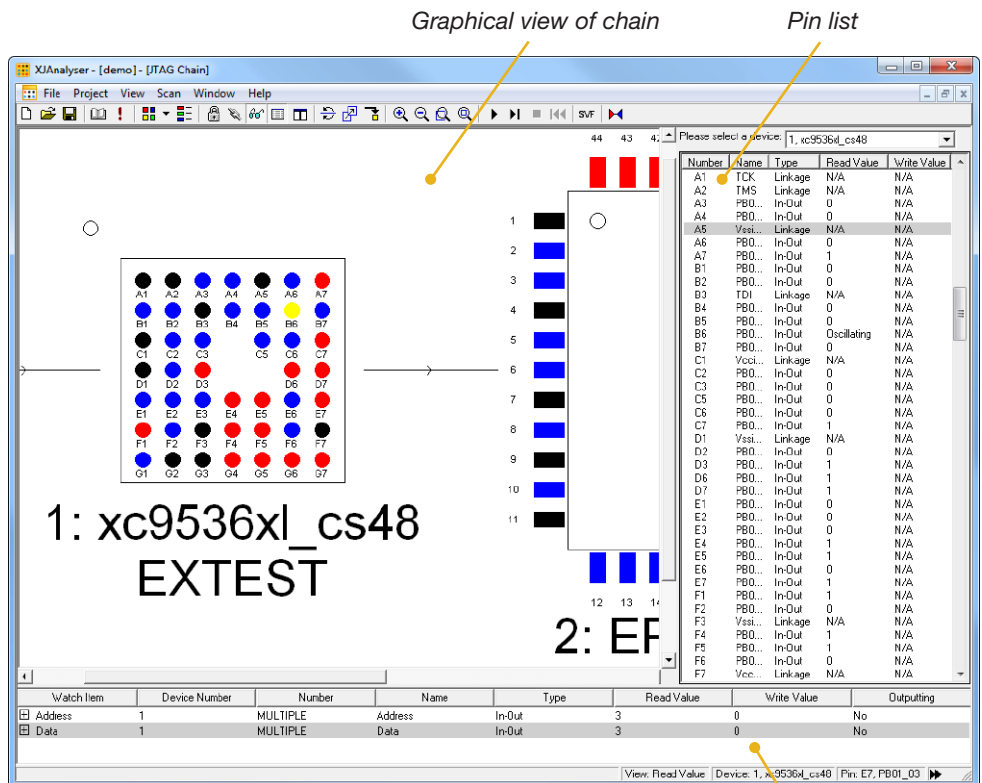
Simplify low-level access to any devices connected to a JTAG device by grouping

Key Benefits

- Allows you to increase yields — by setting pin values and tracing signals you can quickly debug your boards, even under BGAs
- Speed up product development by allowing engineers to debug prototype and development boards in minutes rather than days
- Free up engineering resource by eliminating the need to write functional test software to check fundamental hardware connectivity

pins together into busses (e.g. “Data” or “Address”) and setting values using convenient units (Hex, Binary, Decimal).

Avoid damaging your board — XJAnalyser generates a warning if you attempt to drive any pin to a state that would put it in conflict with a value being driven to that net from a different source.



The screenshot shows the XJAnalyser interface with three main components highlighted:

- Graphical view of chain:** A grid of pins labeled A1 through G7. A zoomed-in view of a specific device is shown below, labeled "1: xc9536xl_cs48 EXTEST".
- Pin list:** A table listing pins with columns for Number, Name, Type, Read Value, and Write Value. Pin E7 is highlighted.
- Watch window:** A table at the bottom showing watch items for Address and Data.

Number	Name	Type	Read Value	Write Value
A1	TCK	Linkage	N/A	N/A
A2	TMS	Linkage	N/A	N/A
A3	PB0...	In-Out	0	N/A
A4	PB0...	In-Out	0	N/A
A5	Vsst...	Linkage	N/A	N/A
A6	PB0...	In-Out	0	N/A
A7	PB0...	In-Out	1	N/A
B1	PB0...	In-Out	0	N/A
B2	PB0...	In-Out	0	N/A
B3	TDI	Linkage	N/A	N/A
B4	PB0...	In-Out	0	N/A
B5	PB0...	In-Out	0	N/A
B6	PB0...	In-Out	Oscillating	N/A
B7	PB0...	In-Out	0	N/A
C1	Vcc...	Linkage	N/A	N/A
C2	PB0...	In-Out	0	N/A
C3	PB0...	In-Out	0	N/A
C5	PB0...	In-Out	0	N/A
C6	PB0...	In-Out	0	N/A
C7	PB0...	In-Out	1	N/A
D1	Vsst...	Linkage	N/A	N/A
D2	PB0...	In-Out	0	N/A
D3	PB0...	In-Out	1	N/A
D6	PB0...	In-Out	1	N/A
D7	PB0...	In-Out	1	N/A
E1	PB0...	In-Out	0	N/A
E2	PB0...	In-Out	0	N/A
E3	PB0...	In-Out	0	N/A
E4	PB0...	In-Out	1	N/A
E5	PB0...	In-Out	1	N/A
E6	PB0...	In-Out	0	N/A
E7	PB0...	In-Out	1	N/A
F1	PB0...	In-Out	1	N/A
F2	PB0...	In-Out	0	N/A
F3	Vsst...	Linkage	N/A	N/A
F4	PB0...	In-Out	1	N/A
F5	PB0...	In-Out	1	N/A
F6	PB0...	In-Out	0	N/A
F7	Vcc...	Linkage	N/A	N/A

Watch Item	Device Number	Number	Name	Type	Read Value	Write Value	Outputting
Address	1	MULTIPLE	Address	In-Out	3	0	No
Data	1	MULTIPLE	Data	In-Out	3	0	No

CPLD programming

You can run STAPL /JAM and SVF files within XJAnalyser. These files are typically used to program devices such as CPLDs and FPGAs. Even if these files were created for a JTAG chain containing just a single device, XJAnalyser can run them on chains containing more devices.

Golden board comparison

You can capture the values being driven onto the JTAG devices of a known good working board. These values can

then be used to identify differences between boards exhibiting unexpected behaviour and a known good board.

Fast, simple setup

XJAnalyser has a simple four-click setup wizard to let you start testing and debugging your board straight away. All you have to do is select a JTAG header and a library containing appropriate BSDL files and you can start working.

Even if you don't have a BSDL file, XJAnalyser will still work with the other devices.

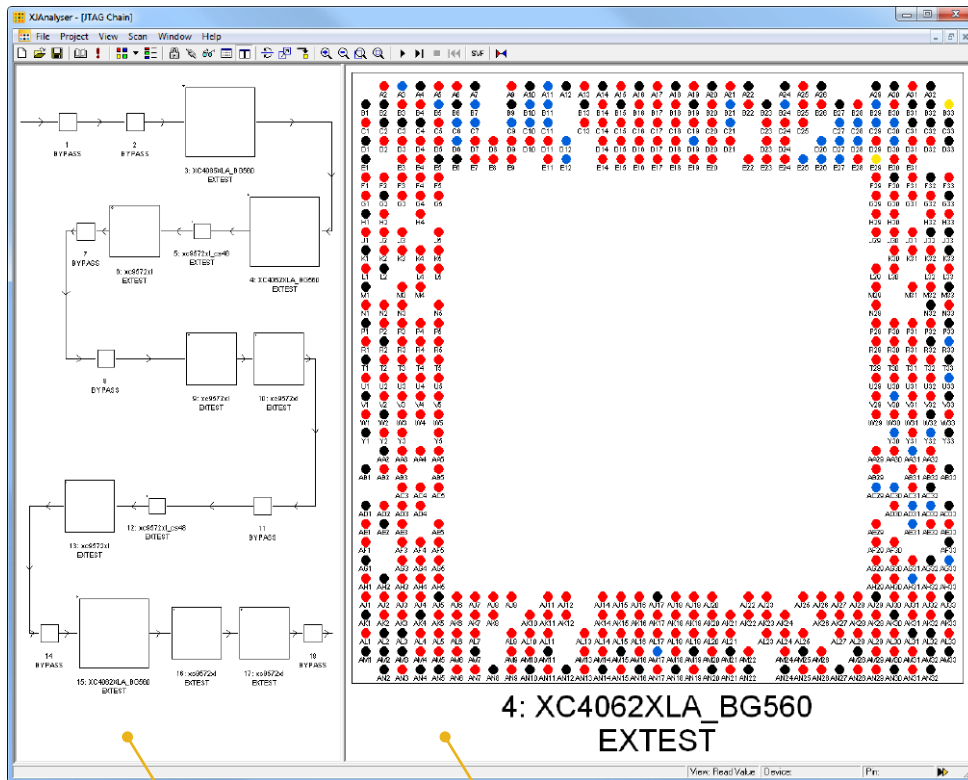
Features

- Able to test BGAs and fine-pitch devices
- Only BSDL files required to get the board up and running
- Set up pin states — e.g. low, high, toggling
- Trace shorts, opens and other signals
- Easy low-level access to device pins/busses
- Clear display of the pins/balls with variable zoom levels and split screen
- Quickly find and monitor changing pins
- Program devices with SVF and STAPL files
- Plug and play
- Real-time interaction

XJTAG gives you more...

XJAnalyser also includes all of the following:

- XJLink — the USB 2.0 to JTAG interface required to connect your PC to the circuit under test
- The licence is held within the XJLink so you can install the software on any number of PCs
- Demonstration hardware with full tutorial
- Support and upgrades for one year



Zoomed out view

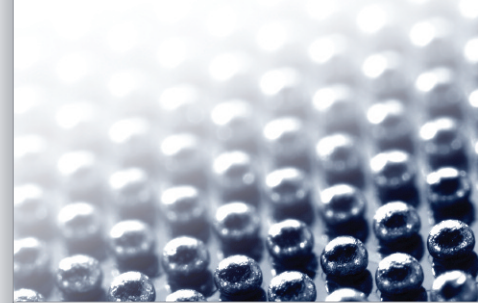
Zoomed in view

opinion

Anthony Merry
Chief Technical Officer
Haliplex

“XJTAG saves us over US\$100,000 per year by reducing the engineering time to commission new boards, enabling us to repair boards more quickly, and reducing the number of boards that are scrapped.”

“Other systems tend to hide details, which makes it difficult to be sure that certain aspects are covered. XJTAG combines powerful capabilities with an extremely competitive price, and represents outstanding value among boundary scan test systems.”



Distributor / Technology Partner