

Overview

The Layout Viewer allows you to quickly find the physical location of components, nets and pins on a board. It provides the capability to view layout design data extracted from ODB++ jobs in both XJDeveloper and XJRunner.

You can use the Layout Viewer to visualise any faults that are found when running tests. The Connection Test output includes clickable links to directly display all of the relevant circuit elements.

Included free with XJDeveloper and XJRunner

The Layout Viewer is integrated into XJDeveloper and XJRunner to help engineers quickly identify faults.

Visualise circuit elements

The advanced graphical display highlights selected components and nets. Individual layers can be turned on or off as required to make it easy to see specific circuit elements.

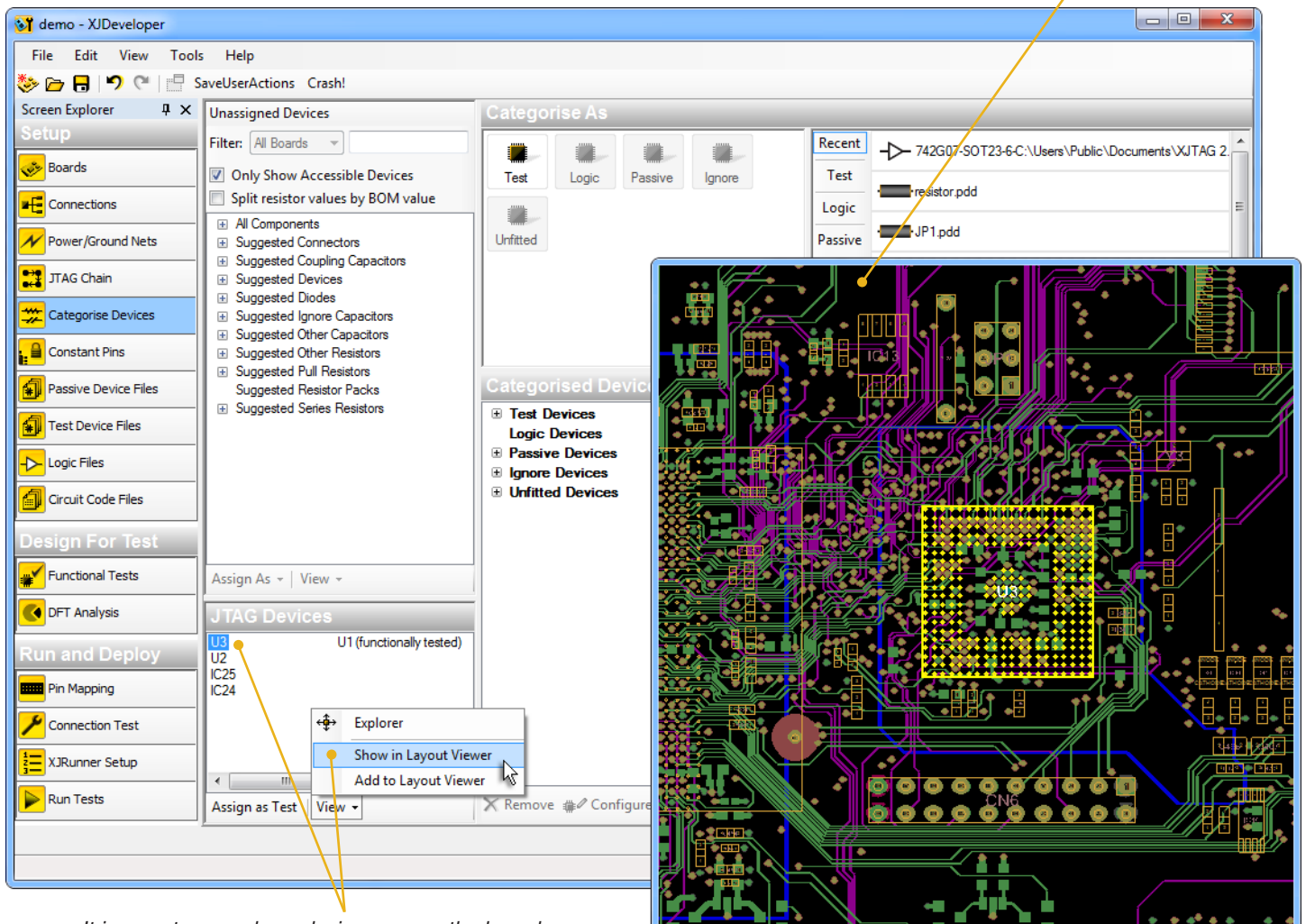
Key Benefit

Improve productivity by visualising the exact location of faults to be repaired

Features

- Aids identifying likely points of failure
- Measures distance between objects
- Control over which layers are visible
- Advanced layer and zoom controls
- Exports graphics to the clipboard, a file or printer
- Import pictures for clearer display

Layout Viewer shown by XJDeveloper



It is easy to see where devices are on the board

Determine the location of faults within seconds

The Layout Viewer can be used to quickly locate where faults are on the board under test.

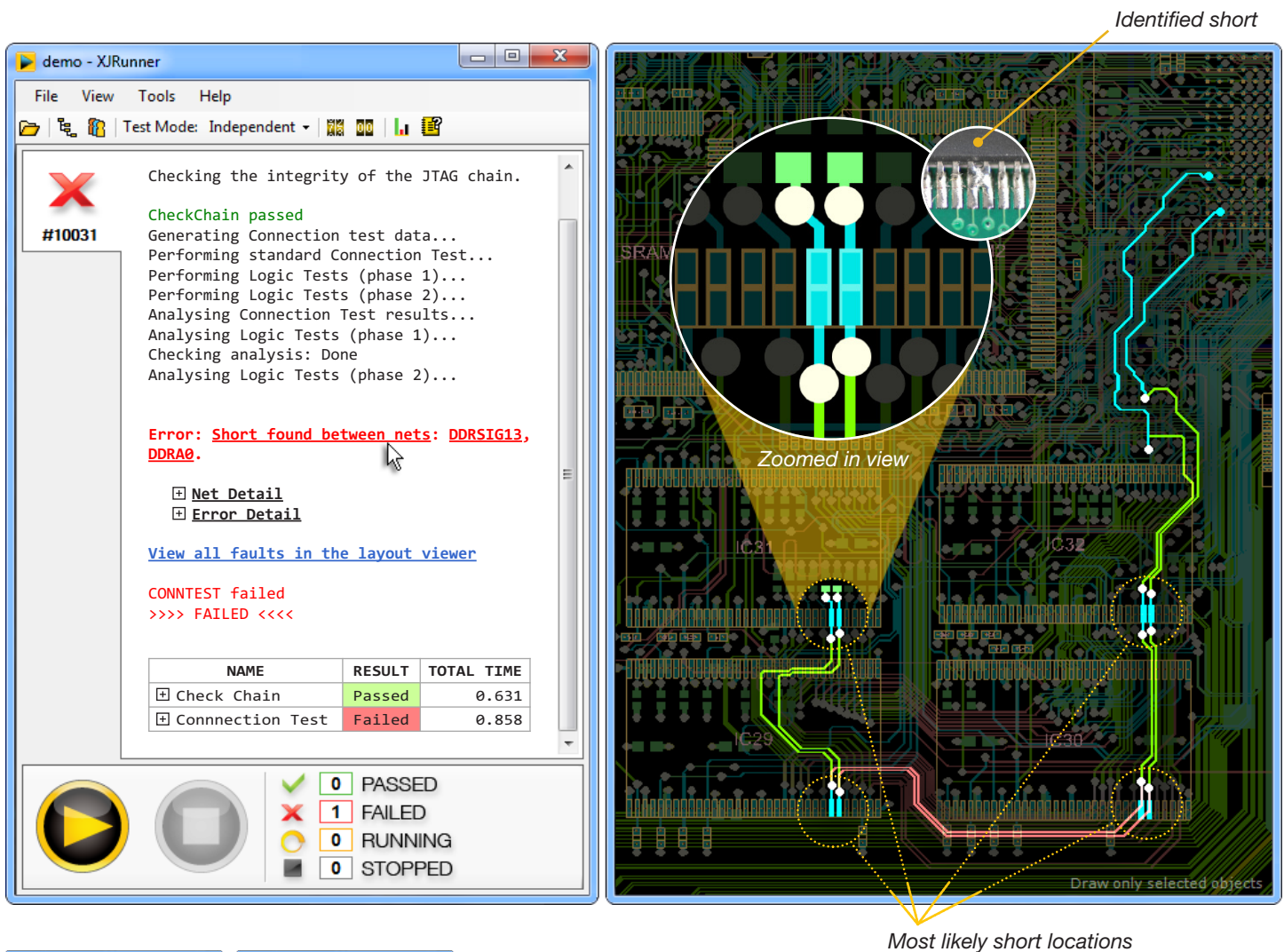
XJRunner's textual output provides details about the types of fault and which nets are involved. There are also clickable links that allow the fault to be easily visualised in the Layout Viewer.

By showing the routing of nets, the Layout Viewer helps to locate the fault on the physical board by showing the potential problem areas.

In the example below, XJRunner reports that Connection Test has failed, and has identified two nets that are shorted together. By looking at the layout, it is

easy to determine that the four most likely locations are the pads on the memory devices. It is unlikely that the fault is under the BGA device as the pins are not next to each other.

By examining the four locations on the board, it was quickly identified that the problem was a soldering fault on IC31.



demo - XJRunner

File View Tools Help

Test Mode: Independent

X #10031

Checking the integrity of the JTAG chain.

CheckChain passed

Generating Connection test data...
 Performing standard Connection Test...
 Performing Logic Tests (phase 1)...
 Performing Logic Tests (phase 2)...
 Analysing Connection Test results...
 Analysing Logic Tests (phase 1)...
 Checking analysis: Done
 Analysing Logic Tests (phase 2)...

Error: Short found between nets: DDRSIG13, DDRA0.

[Net Detail](#)
[Error Detail](#)

[View all faults in the layout viewer](#)

CONNTEST failed
 >>> FAILED <<<<

NAME	RESULT	TOTAL TIME
Check Chain	Passed	0.631
Connection Test	Failed	0.858

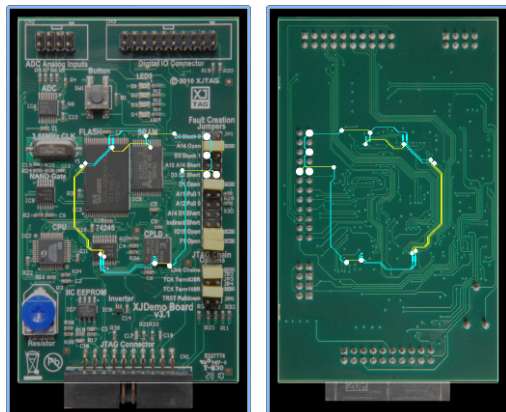
0 PASSED
 1 FAILED
 0 RUNNING
 0 STOPPED

Identified short

Zoomed in view

Most likely short locations

Draw only selected objects



Import board pictures

For even more help in identifying where on a board the faults are located, pictures of the front and the back of the board can be imported.

These images can then be displayed behind the CAD data with its highlighted components and nets.

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