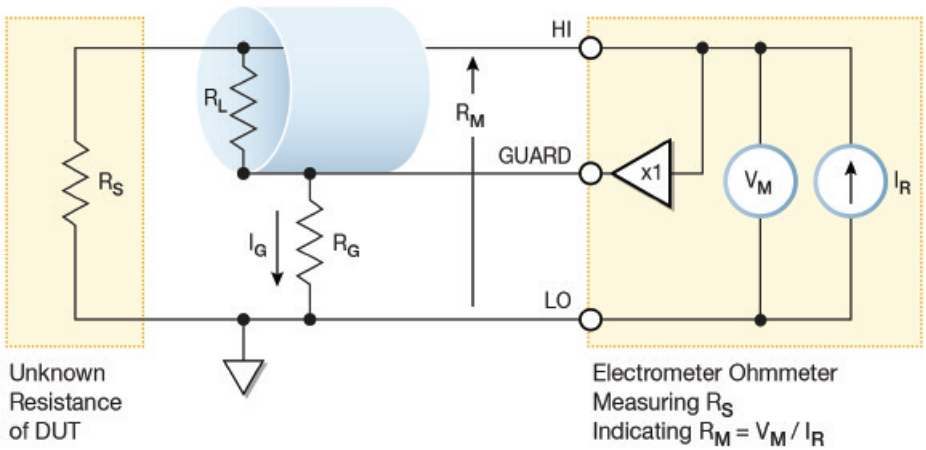
Figure 1: Resistance measurement using the Guarding technique



COMBINING JTAG BOUNDARY SCAN WITH FUNCTIONAL TESTING

By Gian Luca Pizzocolo, Chief Engineer for Research & Development at IPSES, and Dr Bob Storey, Principal Software Engineer at XJTAG

Testing of medium-complexity printed circuit boards (PCBs) at the end of production has traditionally been carried out using in-circuit testing (ICT) and functional testing. Other test methods, such as costly optical and X-ray inspection, are often necessary to verify that BGAs are correctly placed. JTAG boundary scan however, can replace ICT as the natural counterpart to functional testing and make optical and X-ray inspection unnecessary.

ICT AND FUNCTIONAL TESTING

ICT is a method which tests each component or connection in isolation, using methods such as the Guarding technique (see Figure 1) for simple analog components. Access to nodes on the surface of the device under test (DUT), either via a bed-of-nails or flying probe, is used to verify the correctness of the installed components connected to those nodes.

While this type of test verifies the correctness of each individual component, it is unable to verify that the board, once powered, will work properly as a whole unit. To do this it is necessary to perform a functional test (see Figure 2).

Despite the proliferation of new testing techniques, functional test has remained the mainstay for confirming the proper operation of electronic systems and boards. Conceptually, this type of test is simple – it aims to prove that the DUT actually does the job it was designed to do. A bed-of-nails fixture can also be incorporated to provide test access. Use of this test method alone is somewhat limiting, as it can only confirm that each system is operating correctly, rather than evaluate individual components in isolation.

> *"Boundary scan, following the IEEE 1149.x standard, provides circuitry within the chip that makes a comprehensive digital testing protocol available at board level"*

One of the characteristics of functional testing is that it can require the integration of several instruments on the test platform. Suppose, for example, you needed to test a board designed for processing and wireless communication. To perform a functional test you will need other instrumentation such as power supplies, digital and analog I/O, instruments for RF analysis (spectrum and vector analyzers, transceivers, etc.), and fast acquisition devices (oscilloscopes and digitizers) in connection with the test fixture in order to stimulate and read individual signals.

The difference between ICT and functional testing is perhaps best demonstrated with an example. Consider a MAX202 driver for serial interface (see Figure 3). While ICT may be concerned with checking the values of the capacitors in the charge pump, confirming that each component is working correctly in isolation, the functional test would check the sending and reading of entire data packets.

Until recently, ICT has allowed easy verification of the proper installation of all components before the functional test. However, the increasing density of components achievable these days means that PCB designs often do not permit a sufficient number of test points. The pins on BGA components in particular are completely inaccessible to ICT once soldered down. The result is that ICT is becoming less cost-effective and more unsustainable, and lengthens product lead-times. The most appropriate solution to this problem is JTAG boundary scan.

JTAG BOUNDARY SCAN

JTAG boundary scan is an electronic test method designed to overcome problems in test access that are generally associated with complex, high-density boards. Boundary scan, following the IEEE 1149.x standard, provides circuitry within the chip that makes a comprehensive digital testing protocol available at board level.

This circuitry replaces the physical probe points used in ICT with boundary scan cells, located between the core logic of the device and the external pins, which can capture or drive signals for each input and output on the chip.

Boundary scan cells can provide virtual probe points in places a physical probe cannot reach, such as the solder ball connections beneath a BGA. Some fine-pitch leaded devices cannot be reliably tested using a physical probe, but boundary scan can provide digital test access to these pins.

In normal operation of the device, the boundary scan cells are transparent. They capture the values that pass through them, making it possible to observe the flow of data, but not change them. When the correct series of instructions is sent to the control pin (Test Mode Select, or TMS), the boundary scan cells can also drive values out through the pins they are connected to, stimulating the circuit in the same way a physical probe point or nail would. This allows engineers to verify proper interconnection of all the components (the absence of short circuits among the tracks and continuity verification), as well as the proper behaviour of those devices, in the same way that an ICT test would.

The boundary scan cells form a serial scan path known as the'boundary scan register'. A series of values to write can be clocked into this register through the Test Data In (TDI) pin, and once data has been captured by the boundary scan cells, this can be clocked out through the Test Data Out (TDO) pin. JTAG devices can be linked together to form a JTAG chain. The TDO pin from one device in the chain is connected to the TDI pin of the next device, to form a single register. The control and clock signals (Test Mode Select, TMS, and Test Clock, TCK) are common to each device in the chain.

Thanks to this, ICT can be replaced partly or completely with less invasive boundary scan tests, using the boundary scan cells in place of physical nails. Each JTAG chain requires an appropriate Test Access Port (TAP), consisting of four pins (TDI, TDO, TMS and TCK, with an optional fifth – Test Reset, TRST – pin), on an external connector. This connects to a JTAG controller, often a small piece of USB hardware that accompanies the boundary scan software package.

While JTAG boundary scan is found to improve overall test access and therefore coverage, it is a digital protocol, and as such cannot directly test analog parts. Boundary scan access is limited to nets with (and components connected to) at least one JTAG device. Many leading JTAG boundary scan systems include "Design for Test" tools that can show test coverage for a board during the design process, highlighting areas of the board with insufficient JTAG access. At this stage, it may be possible to replace a device that does not support JTAG with one that does, increasing test coverage.

NEW APPROACH: COMBINING FUNCTIONAL TESTING AND BOUNDARY SCAN

In order to comprehensively test a system, boundary scan tests must be run in conjunction with functional tests. When combining ICT and functional test (the most commonly practiced end-of-production tests), engineers will almost always find themselves testing at two different workstations.

Since only four TAP pins on a single connecter are needed for each JTAG chain, it is very easy to integrate boundary scan into a functional test fixture (see Figures 5 and 6) and save valuable time and effort. Some electronics test specialists have actually begun developing fixtures and test benches that integrate both functional and boundary scan into a single workstation, providing more complete devices with competitive overall costs and development times.

MAXIMUM EFFECTIVENESS

The combination of functional and boundary scan test on a single system leads to numerous and considerable benefits. Both methods complement each other, resulting in increased reliability and effectiveness. Using the two together, it is possible to create favourable test conditions otherwise impossible to achieve.

For example, through the stimulation of the probe intended for functional test, it is possible to generate patterns that can be verified by the boundary scan chain and activate parts of the circuit that are then verified by functional test. The effectiveness of this integrated approach means that not only two types of test can run from a single device, but that these tests give greater confidence in the design and manufacture of the board.

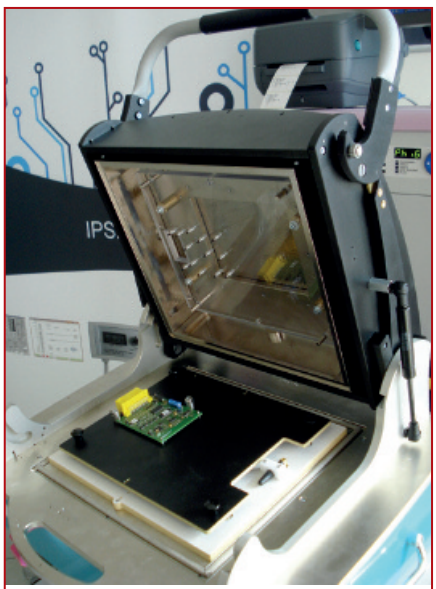


Figure 2: A typical functional test fixture

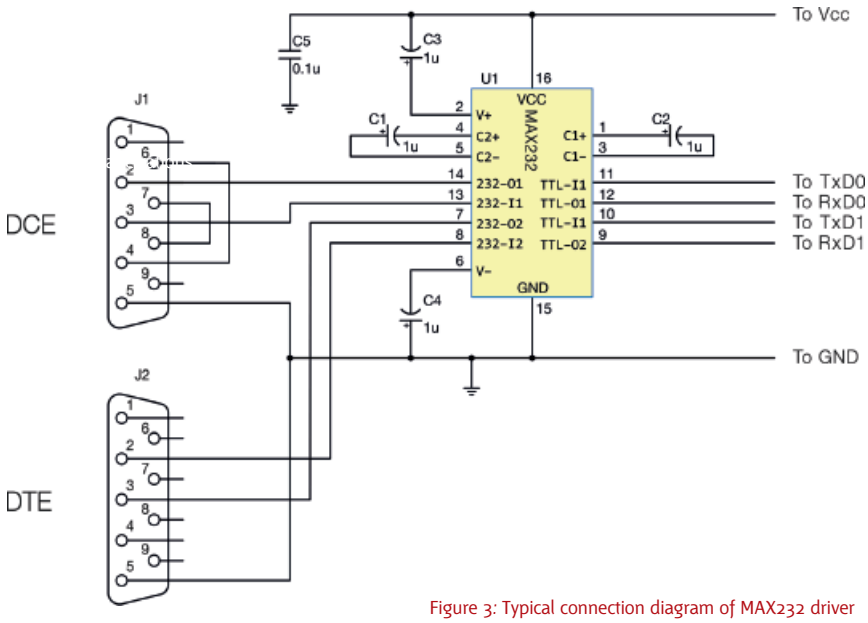
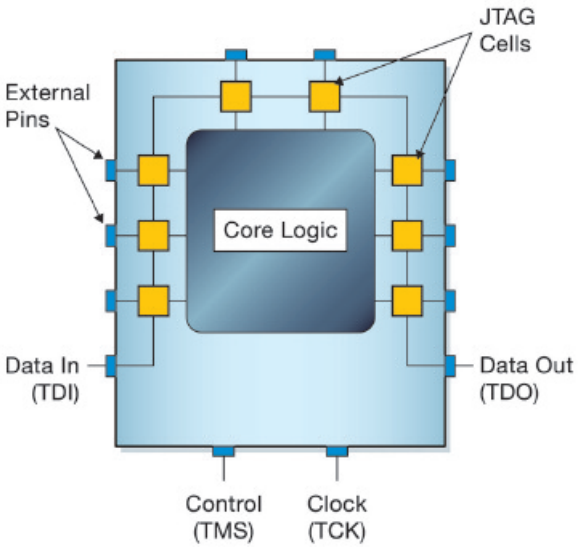


Figure 3: Typical connection diagram of MAX232 driver

Figure 4: Simplified diagram of a boundary scan component



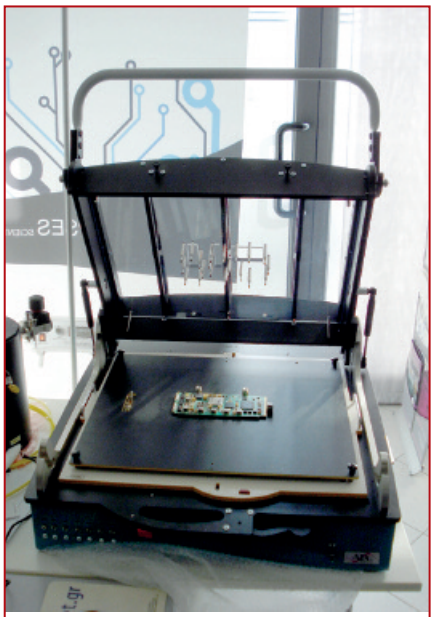


Figure 5: Integrated functional test and boundary scan test fixture with the DUT inserted

A simple example of these benefits can be seen by testing a digital-to-analog converter (DAC) connected directly to an FPGA. Using boundary scan it is possible to properly drive the I/O of the FPGA to program the analog output of the DAC, which can then be measured by an acquisition board through functional test.

On the other hand, if we consider an ADC interfaced directly to an FPGA, it is possible to stimulate the former during the functional test using a generation card and check the bits encoded by the ADC reading the FPGA using boundary scan.

The above integrated approach allows engineers to achieve:

- Full or near-full coverage of all the circuits on the DUT (analog and digital) and of all nets;
- Shorter test time – beside the fact that boundary scan and functional test sequences will be executed in parallel, it is also necessary to consider time spent loading and unloading of the DUT on the test bench, which obviously doubles when there are two workstations;
- High performance in-system programming;
- Faster, more accurate fault diagnosis.

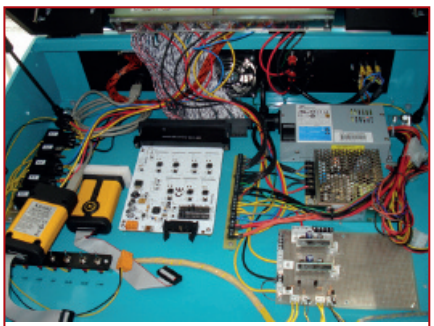


Figure 6: Interior of the fixture, in which both devices for functional test and interface for testing with boundary scan are integrated

For the development of integrated test systems there are now available powerful tools that allow having both, the necessary hardware for interfacing and the development environment for the execution of test sequences. PXI JTAG boards allow interfacing to the boundary scan chain simply by entering the module within a PXI rack, equipped with several hardware modules suitable to the specific application of functional test.

Although development of a boundary scan test sequence should be carried out with the specific tool (a JTAG developer environment), the generated sequence can not only be associated with the sequence developed for the functional test, but you can jointly manage the parts of the sequences that provide the interaction between the two types of tests. In this way, once functional and boundary scan sequences are developed and then integrated, the operator interface will be uniquely customized.

By choosing a modular test system that allows for easy integration of different types of hardware, including that developed by third parties, you can have an easily upgradeable and configurable single bench that integrates functional and boundary scan testing, improving not only the reliability of the tests, but their cost and duration. ●

WHAT IS BOUNDARY SCAN?

Advances in silicon design such as increasing device density and more recently BGA packaging have reduced the efficacy of traditional testing methods. In order to overcome these problems, some of the world's leading silicon manufacturers combined to form the Joint Test Action Group (JTAG).

The findings and recommendations of this group were used as the foundation for the IEEE standard 1149.1, '*Standard Test Access Port and Boundary Scan Architecture*'. This standard has retained its link to the group and is commonly known by the acronym JTAG.

JTAG boundary scan is a test technology designed to overcome the kind of test access problems generally associated with complex, high-density boards. By stimulating boundary scan cells, located on components such as FPGAs and CPLDs, engineers can digitally test the circuits with a JTAG controller and use powerful software packages to pinpoint precise locations and causes of faults.

Since test points are no longer necessary, the physical access problems associated with ITC and functional test are no longer an issue. The test system and boundary scan cells are connected only by means of a 4-5 wire test bus, which must be included in board design to ensure testability. Many leading vendors of JTAG boundary scan systems supply '*Design for Testability*' guidelines to encourage design engineers to do so.

HOW DOES IT WORK?

All the signals between the device's core logic and the pins are intercepted by a serial scan path known as the Boundary Scan Register (BSR). In normal operation these boundary scan cells are invisible. However, in test mode the cells can be used to set and/or read values. A series of 4-5 different signals are used during boundary scan to report back on the circuit's performance.