Boundary Scan Test for FPGA-Based Embedded Design

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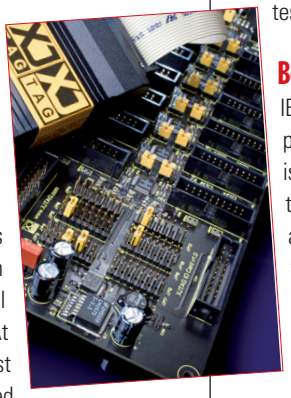
System features integrated into modern FPGAs allow designers to implement an increasing proportion of an embedded design in a small number of reconfigurable components. It is quite normal to take advantage of the FPGA's reconfigurability to download test programs to exercise various parts of the system and to perform self-test routines in the field. During development and prototyping, however, engineers must debug hardware before functional tests are ready. But the presence of the system features that are so valuable to the end product increasingly rules out the use of conventional probe-based test techniques.

Test Challenges

FPGA vendors are penetrating system-level designs with high-gate-count devices that feature high-speed memory interfaces, multiple power domains, embedded CPUs and DSP cores, large internal memory blocks including flash memory, and high-speed I/O transceivers meeting industry standards such as LVDS and gigabit serial I/O. As a result, FPGA images are complex, sometimes comprising several million gates, and inter-IC signal speeds are increasing. At the same time, the largest FPGAs are typically offered in BGA packages that may have more than 1700 pins.



The test access challenges presented by large BGA FPGAs are compounded by multi-layer boards that route inter-IC signals several layers beneath surface. As there can be many thousands of such signals in a modern system design, adding extra routing and vias to bring these to the surface to enable physical probing can introduce undesirable effects.

These factors are diminishing the ability of conventional probe-based test methods to provide a suitable means to test modern embedded boards at the prototype stage and throughout development and production. As a response to this, various methods have been used to embed test routines at the board and system levels, for example by storing embedded test code in the CPU flash memory or by downloading embedded tests for execution in the FPGA. Typically, this has required engineers to develop functional diagnostic code to test the integrated systems.

Downloading test routines to the FPGA is an effective technique for functional tests and performing self-test routines in the field, particularly after an in-system upgrade has been applied. But the tests themselves may not be available until relatively late in development, as test code generation is not automated and the requirements on functional tests are likely to change throughout the earlier stages of the project.

Executing embedded test code also requires the system to be able to function, at least partly. Engineers need a test solution that is not dependent on physical access for test probes, not compromised by high off-chip signal speeds, not subject to delays in test code generation and does not require the board to be able to start-up before even basic debugging can begin. Boundary scan testing potentially represents a solution.

Boundary Scan in Embedded Design

IEEE 1149.1 defines a four-wire test access port and boundary scan architecture, which is implemented in the silicon of the device to be tested. This interface can be viewed as a general-purpose serial communication port, allowing values to be read into and out of internal registers, memories and gates in devices such as FPGAs, EEPROMs, SRAMs or Flash memory.

The test ports of all such devices in the system are interconnected at the board level, setting up a serial scan chain that can be accessed via a single connector at the edge of the board. By manipulating the scan chain to set up suitable test patterns, it becomes possible to stimulate the device core, drive and sense device outputs, and to sense inputs. When the board is functioning normally, the boundary scan circuitry is disabled.

As the numbers of JTAG-compliant devices per board increases, emerging JTAG testers can access a greater proportion of the total nets, thereby increasing overall test coverage. Moreover, responses can also be collected from components that do not offer a boundary scan test interface, provided the device is connected to the same net as a compliant device. This is sometimes referred to as cluster testing, and allows devices such as external connectors, video chips, IIC devices, Ethernet controllers, LEDs or switches to be tested as part of the boundary scan routine.

Modern Boundary Scan Tools

The XJTAG boundary scan development system is designed to enable engineers to significantly reduce the time and cost of board development and prototyping. It features a graphical user interface, which is able to present scan test results in a convenient format that can be interpreted easily and intuitively. Opens, bridges and stuck-at faults present on inaccessible nets, for example, can be located as easily as using a logic analyser or oscilloscope, without requiring the system to start up.

The XJTAG system also allows engineers to step through or over the test code a line at a time, edit and display breakpoints, and check or modify the values of any variables in the code. By using the XJTAG digital I/O card it is also possible to enhance functions such as cluster testing of non-JTAG devices by manipulating I/Os to eliminate the need for loop-backs, cable swapping and costly custom test jigs to test devices with large numbers of I/Os.

JTAG compliant devices are provided with an appropriate Boundary Scan Description Language (BSDL) file, which describes how to manipulate the internal circuitry when the device is in boundary scan mode. The XJTAG system combines the BSDL files for the components on the board with the board netlist and a test script written by the engineer that describes how the device is to be tested. The script is written in an intuitive high level language, which is therefore easily readable by electronic designers and software engineers.

The use of a high level language abstracts engineers from the intricacies of the boundary scan data stream. This supports fast test development, eliminates human error, and facilitates development of sophisticated test routines that require minimal physical access to the board.

The device-centric nature of XJTAG tests means that a script for a particular device can be stored and re-used at a later date when the same component is designed into a subsequent product. In this way, a device-centric approach to boundary scan testing that facilitates re-use of test knowledge acquired throughout the product lifecycle is achieved. Engineers using this technique are effectively creating test IP that can be used again and again to reduce development costs and turnaround time for a multitude of board and product designs. </End/> **www.xjtag.com**