
# All for one

How the latest Jtag interfaces can be a useful ally in the fight to cut development time. By Mike Richardson.

Whilst the motto, 'all for one, and one for all' is traditionally associated with the Three Musketeers and their loyalty to each other through thick and thin, the same sentiment can be applied to the launch of XJTAG's Version 2.0 boundary scan development system.

The company's latest brainchild aims to give customers an 'all in one' boundary scan system that enables them to get their boards up and running in minutes and hours, not days and weeks as is the case with some traditional systems. The point being made here is that in today's 'right first time' environment, developers increasingly need a test solution that not only maximises test coverage when it come to manufacture, but minimises board debug time in order to get their designs to market quickly. XJTAG says it now provides a common platform that can be shared by 'one and all' during the design and development of the product lifecycle.

"The whole approach is to maximise reuse, so the idea is that when you write the software once, you can use it many times," explained XJTAG's ceo Simon Payne. "The increasing amount of bgas and chip scale devices entering new designs means that board real estate is shrinking whilst densities are getting ever higher. Engineers can no longer afford the luxury of ignoring boundary scan methodology – how else are you going to test these devices? You can't get access to them using an oscilloscope, so this is where boundary scan comes to the fore. Our job is to educate the marketplace and make people aware that Jtag can make their job a whole lot easier."

XJTAG can help you diagnose potential faults even before you've had the board back from prototype manufacture. And when you do eventually get the board, it can help to diagnose faults at this point.

"It's important to remember that the development work you've already done is then encapsulated, so you can use it again and again," advised company cto Dominic Plunkett. "Therefore, you decrease the development time because the work already done can be reused within your organisation. Jtag helps you identify and prevent faults at a much earlier stage in the development cycle. Everyone is trying to get it right first time!"

V2.0 introduces a drag and drop interface that automates the Jtag chain discovery and set up process to save time and hassle. Developers simply connect the

computer to the unit under test via the USB2.0 XJLink hardware module, create a new project and add the target board. Additional boards can be added to the circuit with a couple of extra clicks to form a complete 'system'. The XJTAG system then detects the scan chain and matches the Jtag device codes to their respective BSDL files, as well as identifying ground nets and making intelligent suggestions about other components.

This enables hardware developers to quickly and easily categorise all of the non jtag or cluster devices in the circuit. For example, with one click all the pull resistors or any component type can be grouped together for speed and convenience during the set up stage. XJTAG says that provided you have access through a jtag enable device, you can test non jtag devices seamlessly.

"We're trying to capture as much of the test procedure as possible, including non jtag devices," continued Plunkett. "It's important to remember that new board designs or revisions are often similar to previous ones. With XJTAG, all the developer needs to do is tell the system what

changes have been made and they can simply reuse the test procedure for the next revision of the board.

"For example, if we test a potential non jtag device – say an Ethernet controller – we can send and receive real Ethernet packets without large parts of the system even needing to be fitted to the board. If we know at this early stage in the design cycle that we can send and receive Ethernet packets, then we know the Ethernet interface is working. Later during the development cycle, the software team may question that the hardware is faulty. If this is the case, simply run the same tests again to demonstrate that you can send and receive Ethernet packets. This will tell the software team that it needs to look elsewhere for the problem. It removes those conflicts that might otherwise arise because you are unable to substantiate them."

## All systems go!

XJTAG has also recently added support for Xilinx's Virtex-5 fpga System Monitor to enable customers to check power supplies or perform overall thermal management using the JTAG port on the 65nm Virtex-5 fpgas.

"The System Monitor is an integrated system within the Virtex-5 which allows users to read the fpga's power supply, other analogue inputs and the temperature of the chip," continued Plunkett. "For example, using the System Monitor and XJTAG tools in tandem, users can check their power rails are within tolerance very early in the process - even while it's fully operational. This provides a wealth of information because the user is actually measuring at the die of the fpga, not remotely. Ever increasing processor speeds mean that chips are running hotter, so designers have to be more aware of airflow and heatsinks."

During operation, the design may be operating at a cooler temperature so developers can reduce the amount of cooling their system requires. Equally, if it's running slightly warm, they can concentrate on increasing the cooling of the design.

Plunkett develops the theme: "Normally, the test engineer would need to locate a remote temperature probe within the casework which requires more effort, whereas with the System Monitor you are measuring 'on chip'. You can't do this with a remote temperature probe because you are physically unable to get inside the package. You're not adding any infrastructure to do this with the Virtex-5 System Monitor because it's all done through the jtag interface."

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Simon Payne, **XJTAG**

He goes on to add that although the power supply module may be running the correct voltage elsewhere in the system, through the jtag interface the Virtex-5 System Monitor measures voltage at the die which helps to identify voltage drops across pcb tracks or wires. Furthermore, this can be done whilst the chip is under operation.

XJTAG has quickly recognised the power of what had been added to Xilinx's design capabilities by providing customers with the jtag tools to enable them to use the potential of the System Monitor to its fullest extent. After all, if you want to cut your development time and get your design to market first, you've got to fight for what you want!