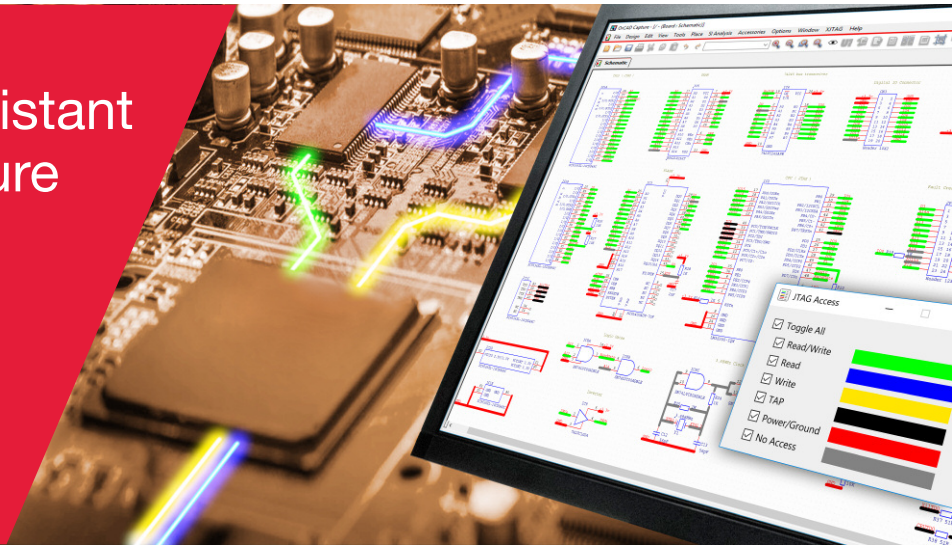
## New XJTAG® DFT Assistant tool for OrCAD® Capture

Free, easy-to-use 'Design for Test' plugin so you can catch errors before layout and avoid costly re-spins

**FlowCAD**




**"Developed by XJTAG, the software for OrCAD Capture will significantly increase the Design for Test and Debug capabilities of the schematic capture and PCB design system."**

**OrCAD Capture has a multitude of features that help engineers manage their PCB designs efficiently, from initial schematic entry through design analysis and rule checking, layout optimisation, component selection and BOM management. Tools such as automated wiring accelerate laborious processes, viewers with colour coding help inspect nets and navigate connection hierarchies, and database and search tools help streamline component selection.**

Engineers now need to be able to determine at the schematic stage how they can best implement Flash programming, JTAG debugging and boundary scan testing. With OrCAD Capture users now have access to XJTAG DFT Assistant to help check that JTAG chains on the board are setup correctly and ready to support testing, debugging and programming. By eliminating errors and helping ensure the JTAG chain is used to its full potential, DFT Assistant helps boost test coverage and ensures that prototype boards can be tested and programmed with boundary scan as soon as they are received back from assembly.

Verifying designs at the schematic stage delivers advantages from the beginning of the product lifecycle. It can help check for errors before any hardware is built. The extra effort really starts to show its value when the first prototype boards are produced enabling connection tests to be done in minutes whereas manual probing can take hours to locate shorts or opens if the board will not start up. Having a working JTAG capability early in the debug stage will enable accelerate board bring up and enable firmware programming and CPU debugging as well as boundary scan testing.

"We saw that our customers could benefit from direct integration of JTAG in OrCAD Capture," comments Kishore Karnane, Director Product Management, Cadence OrCAD Solutions. "XJTAG was the ideal partner to help us achieve this, bringing their specialist knowledge and their expertise in testability issues and design."

The result of this collaboration, XJTAG DFT Assistant for OrCAD Capture, consists of the XJTAG Chain Checker and XJTAG Access Viewer. XJTAG Chain Checker identifies common design issues such as connection errors in the JTAG chain design or incorrect termination of signals at Test Access Ports (TAPs). A single mistake in this area of the product design could prevent the chain from working, so it is vital that checks are done before the PCB is produced.

XJTAG Access Viewer helps engineers assess the testability of their design, and identify where coverage could be improved, by displaying the extent of JTAG access as an overlay on the schematic diagram. A helpful selection tool enables engineers to analyse specific areas of interest easily by displaying the test access to nets (read, write, power/ground or no access) individually or in groups by selecting them using checkboxes. The nets are colour coded by their JTAG access to aid inspection.

Kishore Karnane sums up, "XJTAG DFT Assistant enables us to deliver even greater value for our customers by providing powerful testability analysis. The deep understanding of JTAG / boundary scan and design automation, by XJTAG, has ensured a high-quality solution that enables users of OrCAD Capture to create even better products more quickly and efficiently."

Cadence products are distributed by FlowCAD in Germany, Austria, Switzerland, Poland, Czech Republic, Slovakia, Hungary, Romania, Bulgaria and South Africa. www.FlowCAD.com

## opinion

**Urs Allemann**
**Director Design Services**
**ed electronic design ag**
**Switzerland**

"Wir müssen frühzeitig in der Designphase feststellen, wie die Testabdeckung mit der minimalen Anzahl von Testpunkten maximiert werden kann. Daher ist es entscheidend, zu wissen, welchen JTAG-Zugang in der schematischen Phase zur Verfügung steht. Der XJTAG DFT-Assistent für OrCAD Capture erleichtert es uns, die Testabdeckung bei der Entwicklung des Designs vorauszusehen. So können wir unsere Tests optimieren, bevor die Leiterplatte hergestellt wird."

"We need to determine early in the design phase how to maximize test coverage using the minimum number of test points. So it is vital to know what JTAG access is available at the schematic stage. The XJTAG DFT Assistant for OrCAD Capture makes it easy for us to see the test coverage as the design evolves and this allows us to optimize our testing before the PCB is produced."

## Data Bank

cadence®

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|---|---|
| Company | Cadence Design Systems HQ USA |
| Nature of business | Leading provider of electronic design automation (EDA) tools, software, IP and services |
| Main products | Broad portfolio of tools for the design and verification of chips, packages, boards, entire systems |
| Customers | Global electronic design community |
| Founded | 1988 |
| Employees | 6700+ worldwide |
| Revenues | US $1.7 billion |
| Location | San Jose, California, USA Offices worldwide |
| Web site | www.cadence.com |