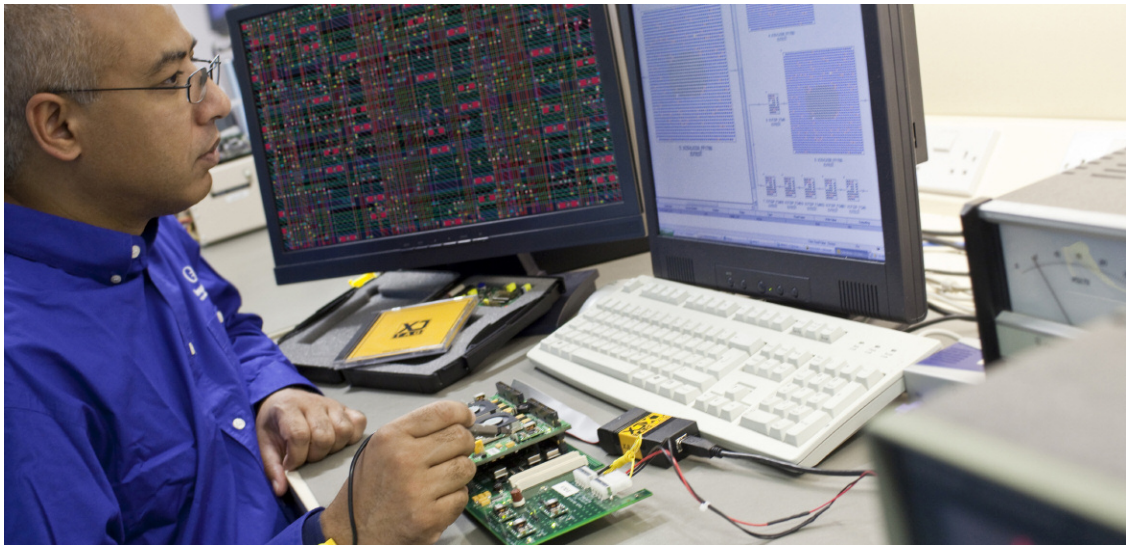
Imagination Technologies



Durgesh Patel, Senior Design Engineer

Mark Dunn, VP Engineering with Simon Payne, CEO XJTAG

Graham Deacon, Director of Verification

Imagination develops SoCs faster using XJTAG boundary scan

"Imagination Technologies, a leading IP innovator, is using XJTAG boundary scan to accelerate development of System-on-Chip designs based on industry-leading multimedia IP. Using the system to debug early test hardware, engineers are able to develop tests even before prototype boards are delivered, and to identify any manufacturing flaws within minutes before commencing design verification."

Imagination Technologies provides comprehensive System-on-Chip (SoC) design services including fully bespoke solutions or standardised platform implementations, based on Imagination's industry-leading IP portfolio. The IMGworks group develops complete SoC solutions using Imagination's IP cores, and works with chip companies as well as leading consumer-product brands targeting mobile- and multimedia-products markets.

"We have developed a state-of-the-art design flow, to provide a fast and low-risk path to production for our customers, says Mark Dunn, VP of Engineering at IMGworks. "Speed is vital, as our customers are typically aiming for a very short market window and rely on us to help them beat their competitors to market."

As a part of its IP development flow, Imagination builds small numbers of boards and test chips for verification purposes, and also produces development systems as necessary for specific customer contracts. The hardware is usually complex, typically having high I/O interconnect density with complex FPGAs and many signals running on internal layers that cannot be probed. "When the first prototypes come back from manufacturing, everything is new: the board, the software, the chip design," explains Graham Deacon, Director of Verification. "Obviously we want to start design verification quickly, so we need a fast way to track down any production defects."

Historically, Imagination's engineers have used socket-based testing to identify hardware faults. This has involved configuring the FPGA to carry out functional tests. Connectivity is very difficult to check in any other way, according to Deacon. In practice, however, significant resources must be committed to develop effective board-level tests by changing the function of the board. "It can involve a couple of weeks of effort," he suggests.

A faster and more efficient approach was needed, but although the team at Imagination had knowledge of various boundary scan test systems, only XJTAG offered the functions and ease of use they were looking for. "XJTAG's engineers demonstrated the system using our own assemblies, which gave us complete confidence that we could quickly produce the tests we need," says Mark Dunn.

Imagination is now using XJTAG to test and debug prototypes, test assemblies and customer development boards. Highlighting the system's convenient and powerful features such as the built-in connectivity test, Graham Deacon explains that connectivity testing and further tests using XJTAG are performed directly after the initial power check on any new board. "XJTAG has significantly reduced test-development effort, and we can compile effective test scripts even before the hardware is ready." Test execution time is usually around 10 minutes, and the tests filter out the majority of assembly flaws, whereas socket-based tests used to take over one hour to execute.

"XJTAG has much greater functionality than we expected. We can test memory interfaces and non-JTAG components well beyond the scan chain. This makes the system very flexible for debugging in the laboratory. It's a powerful engineering tool, which is perfect for our requirements," says Dunn.

opinion

Mark Dunn
VP Engineering, IMGworks
Imagination Technologies

"XJTAG has significantly reduced test-development effort, and we can compile effective test scripts even before the hardware is ready. Testing with XJTAG is our first action after the initial power-up check of a new board, and we are able to test a high proportion of each board for any manufacturing defects within around ten minutes."

"XJTAG has much greater functionality than we expected. We can test memory interfaces and non-JTAG components well beyond the scan chain. This makes the system very flexible in a lab debug environment. It's a powerful engineering tool."

Data Bank

Imagination

Company	Imagination Technologies
Nature of business	Flexible and customizable IP for customer SoC applications
Main product	POWERVR, META, and ENSIGMA IP core technology families
Customers	Consumer electronics markets such as digital radio & audio, mobile phones, personal media players, navigation & driver information, mobile internet devices, digital TV & set top box, mobile TV...
Location	HQ Kings Langley, UK Offices in Far East, India, USA
Web site	www.imgtec.com