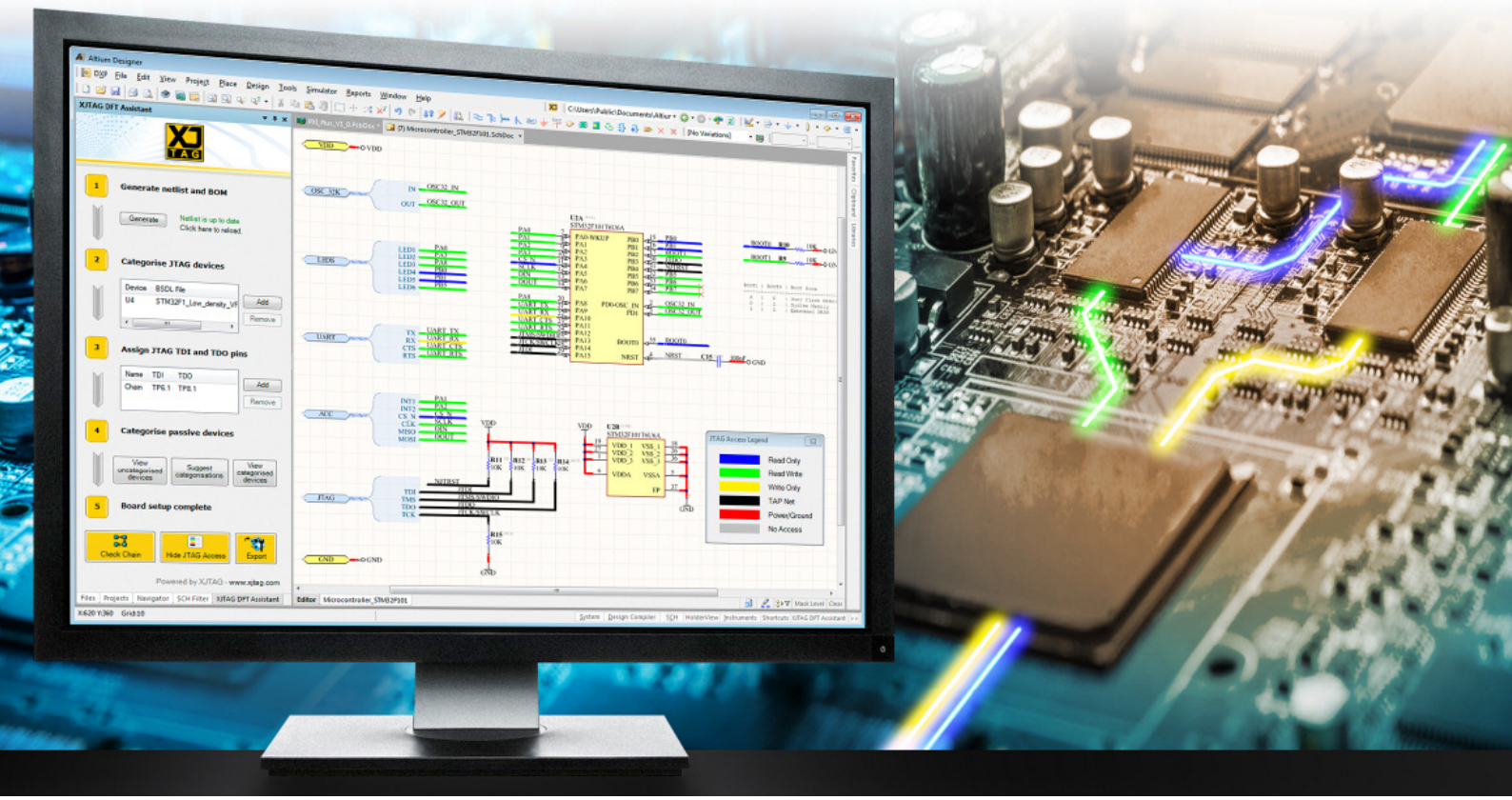
XJTAG® DFT Assistant for Altium Designer®

Installation and User Guide

Version 3



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1. Introduction

XJTAG DFT Assistant for Altium Designer is a *Software Extension* for the **Altium Designer** platform, developed by XJTAG, a leader in JTAG/Boundary Scan technology. The extension provides added functionality to the platform in the form of running Design For Test (DFT) checks on boundary scan chains in a schematic diagram. These checks ensure the scan chain is correctly connected to each JTAG-enabled device in the design, as well as checking that each signal in the chain has been correctly terminated.

The extension is made available free of charge.

Please note, this extension requires Altium 15 or later and is NOT compatible with versions higher than 24.7.
*Visit **www.altium.com/products/downloads***

2. Installation

The extension can be found in the *Extensions & Updates* view within the platform (*see Figure 1*). As this is a free extension, it will automatically appear in the *Purchased* view; if it doesn't appear, use the *Refresh* control at the top-right of the page to refresh the view.

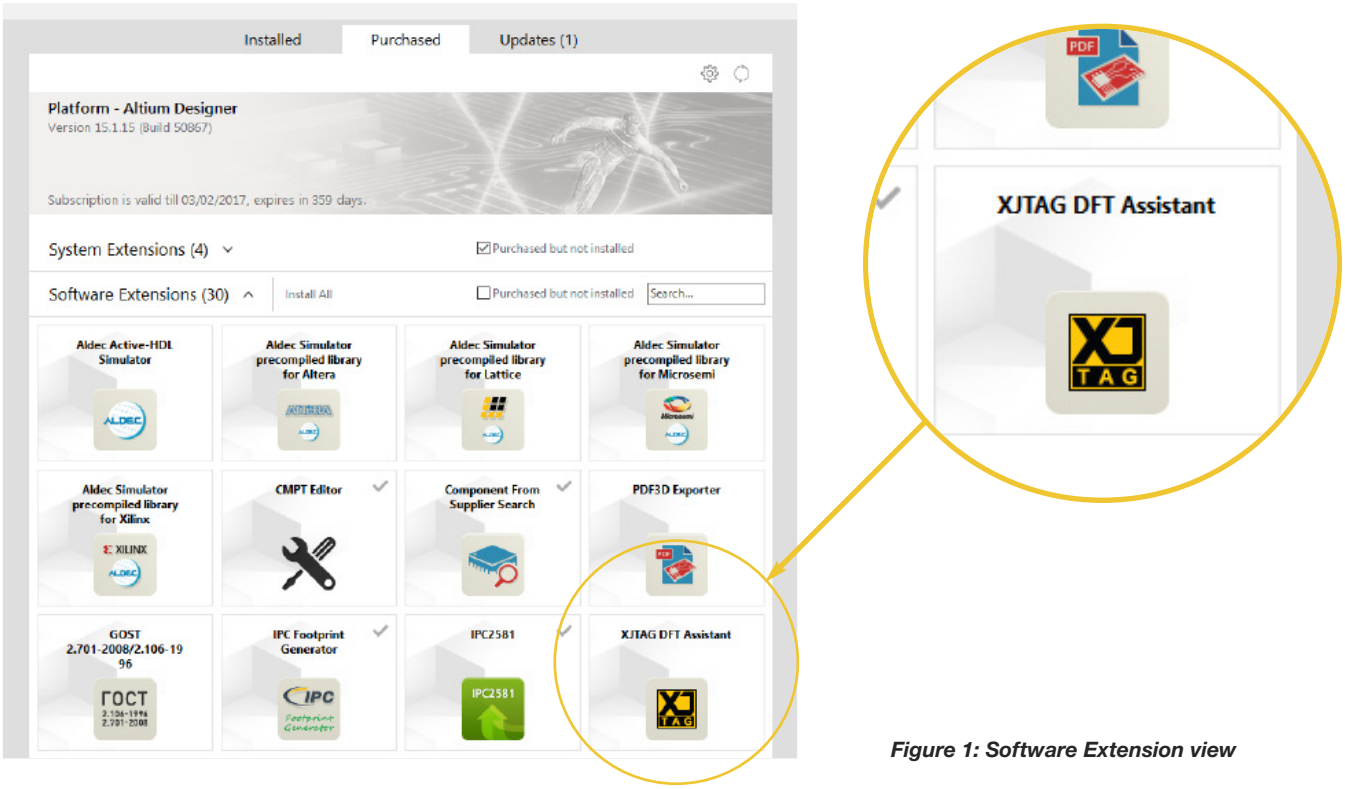


Figure 1: Software Extension view

Unless it is already installed, the **XJTAG DFT Assistant for Altium Designer** extension will appear in the *Software Extensions* part of the view. (Note: disabling the *Purchased* but not installed option in the top-right of the page will show all purchased extensions, including those already installed).

Clicking on the name of the extension will bring up a detailed overview of the extension, showing the publisher (XJTAG), version, release date, its source and a detailed description.

The extension can be installed by either clicking on the *Download from cloud* icon on the summary page, or the *Install* button from the detailed overview page. Installing from the summary page will display a progress bar as the extension is downloaded.

Once downloaded and installed it is necessary to restart **Altium Designer** for the changes to take effect. You will be alerted when the restart is required.

Updates to the extension will appear in the *Updates* view of the *Extensions & Updates* view. As with the initial installation, an Update can be installed from either the summary or detailed overview pages. As with the initial installation, a restart will be required following an update.

3. Quick Start Guide

1. Install the **XJTAG DFT Assistant for Altium Designer** from the *Extensions & Updates* view (*See Section 2*)
2. Open an Altium Designer project with a schematic diagram, or start a new project
3. Open the **XJTAG DFT Assistant** from the *View* menu or click on the XJ icon in the toolbar
4. Assign BSDL files to all JTAG-enabled devices in the design (*See Section 4.3.1*)
5. Define the scan chains and their TDI and TDO pins (up to four scan chains) (*See Section 4.3.2*)
6. Categorise any passive devices in the chain(s) (*See Sections 4.3.3 & 4.3.4*)
7. Run the **XJTAG Chain Checker** (*See Section 4.4)*
8. Run the **XJTAG Access Viewer** (*See Section 4.5*)

4. User Guide

4.1. Background

Boundary scan, as defined by the IEEE 1149.x family of standards, is a technology which enables a JTAG-enabled Integrated Circuit (IC) to relinquish control of its pins to an external agent for test purposes. The logic required to do this is included in the IC at each JTAG-enabled pin, known as a boundary scan ‘cell’. These cells are connected in series within the IC and accessed externally through a 4- or 5-pin port known as a Test Access Port, or TAP.

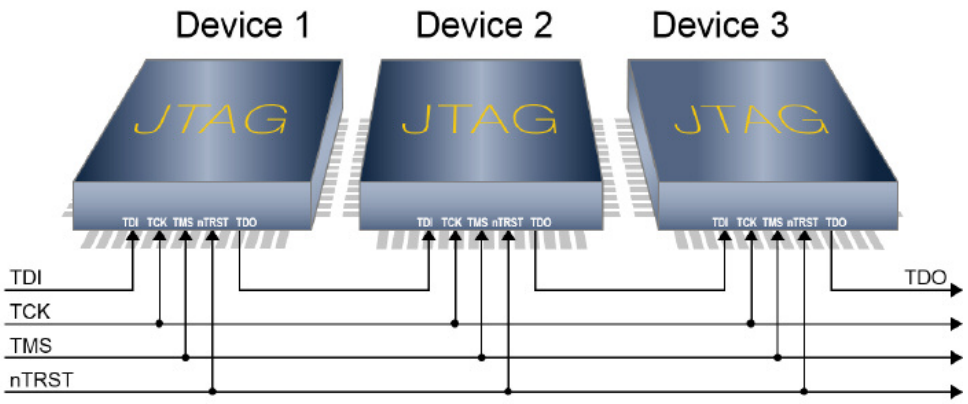


Figure 2: A boundary scan chain connecting three ICs

The TAP on each JTAG-enabled IC can be connected serially creating what is referred to as a boundary scan chain (*see Figure 2*). As each IC is a link in this chain, it is imperative that the chain's integrity is maintained through its entirety; from where it enters the board, to where it leaves. Typically this would be on two pins of the same connector.

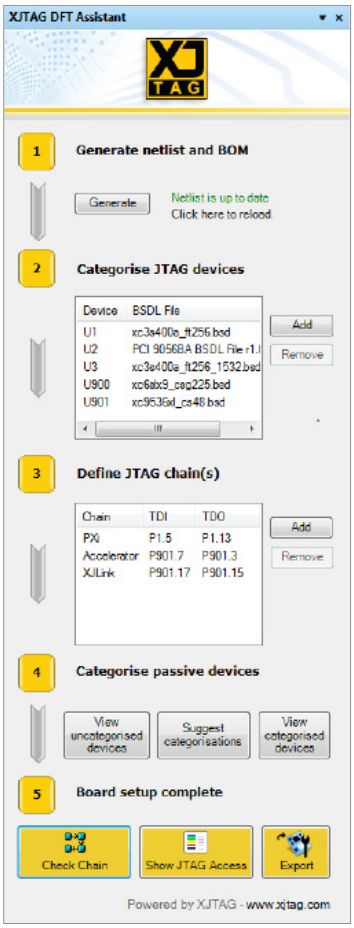
The **XJTAG DFT Assistant for Altium Designer** software extension provides a level of automation in checking that one (or many) scan chain(s) on a PCB are connected and terminated correctly. Crucially, these tests are carried out at the schematic capture stage, thereby identifying errors early in the design cycle and helping to avoid costly PCB respins.

4.2. Setup Overview

Because the software extension is fully integrated into Altium Designer, most of the information needed to conduct a DFT check of a boundary scan chain, such as a netlist and BOM, can be accessed within the platform automatically. However, it is also necessary to provide some additional information that would not normally form part of an Altium Designer project. Specifically, a Boundary Scan Description Language (BSDL) file must be provided for each JTAG-enabled device in the design.

In order to comply with the IEEE standard, it is a requirement for the IC manufacturer to supply a BSDL file for each JTAG-enabled device. Sourcing BSDL files is, therefore, not difficult but it is recommended they be obtained direct from the manufacturer's website in order to guarantee they are the latest versions.

BSDL files can be assigned to ICs using the **XJTAG DFT Assistant for Altium Designer** interface, which can be used as a floating panel or docked to the side of the Altium Designer screen once the extension is invoked from the main menu (*see Figure 3*).



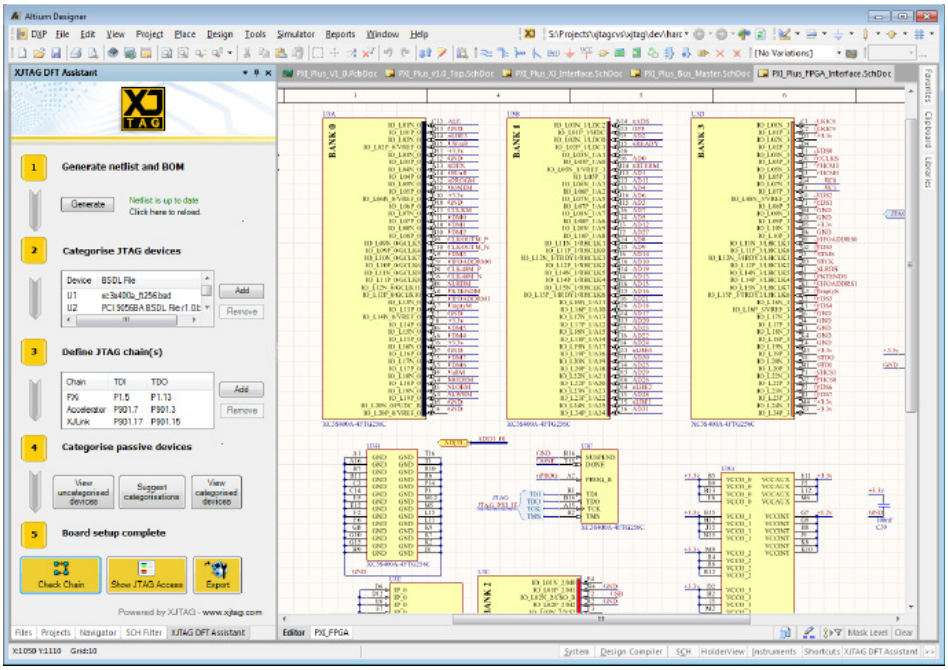


Figure 3: The DFT Assistant User Interface

Once a BSDL file is imported and associated with an IC it is stored as part of the Altium Designer project, so the process does not need to be repeated.

Other non-JTAG devices that may propagate boundary scan access or form a part of the JTAG chain include standard logic and passive devices. The **XJTAG DFT Assistant for Altium Designer** will help identify any such devices in the schematic and allow the designer to categorise them. In addition, pressing the *Suggest Categorisations* button will attempt to auto-categorise any commonly seen components such as series resistors and pull resistors. Any devices not categorised can be assigned later if the project is exported and opened in **XJDeveloper** (*see Section 5.0 for more details*). All categorisation information will also be stored as part of the project.

4.3. Workflow

The **XJTAG DFT Assistant for Altium Designer** panel opens as a new panel in Altium after selecting *Open XJTAG DFT Assistant* from the *View* menu or clicking the icon in the toolbar (*see Figure 4*).

There must be a schematic document open to enable the menu options. When the Assistant panel is opened for the first time, most of the UI will be disabled until a netlist is generated by clicking on the

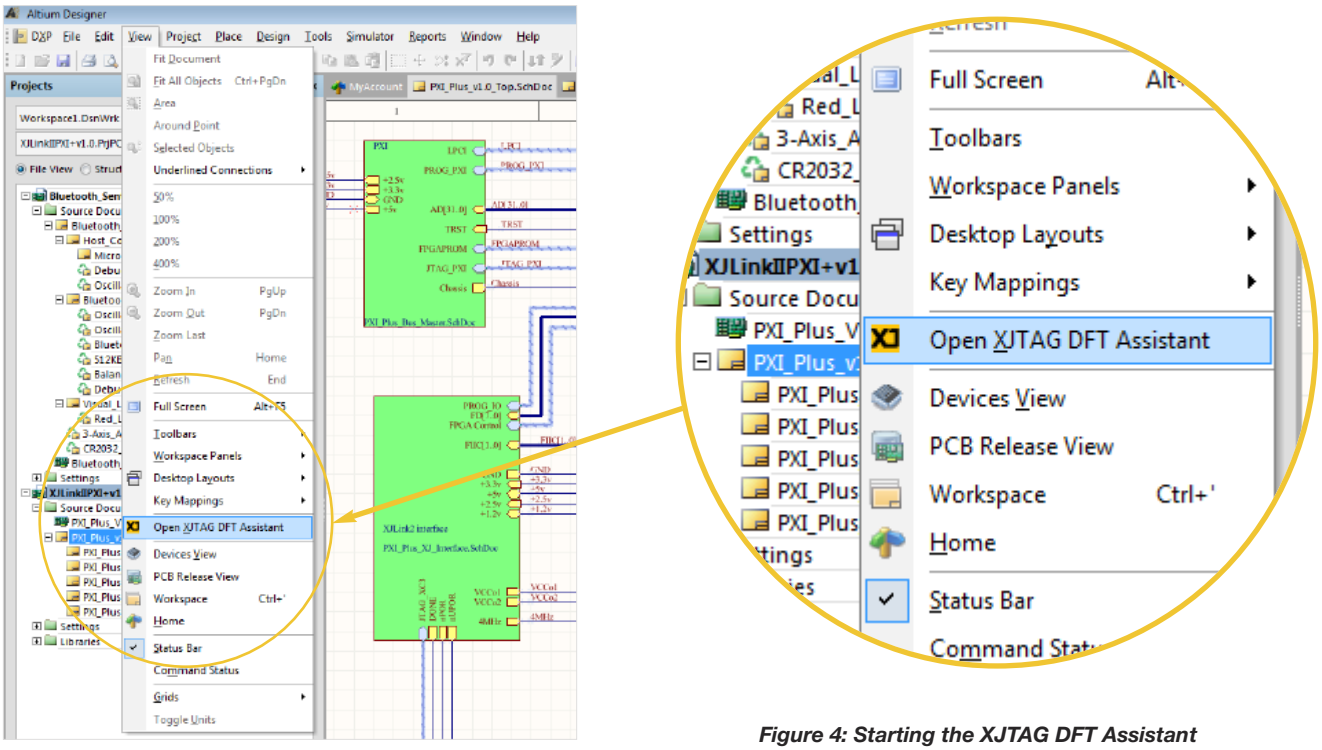


Figure 4: Starting the XJTAG DFT Assistant

Generate button towards the top of the panel. It is a requirement to generate netlist and BOM information for the current Altium schematic project before any DFT analysis can be carried out. If the design is changed while the Assistant is open the netlist should be updated by clicking again on the *Generate* button. This will carry out a netlist update in the background and a progress bar will be displayed while this happens.

There are three stages to performing a board setup:

- Categorise JTAG devices
- Assign JTAG TDI and TDO pins, and
- Categorise passive devices.

These actions can be carried out in any order and will be discussed in more detail below. Once board setup is complete there are three options available to the user at the bottom of the Assistant panel: Check the JTAG Chain, Show/Hide JTAG Access, or export XJDeveloper project.

4.3.1. Categorising JTAG devices

JTAG-enabled devices in the schematic should be identified by the user and assigned a BSDL file. It is recommended to obtain BSDL files from the appropriate part manufacturer's website. To associate a BSDL file with its component, press the *Add* button next to the JTAG devices list view (*see Figure 5*). The *Add JTAG Device* dialog box will open containing a device selector control and BSDL file selector control. Start typing a device reference into the device box and it will provide suggestions for devices in the circuit.

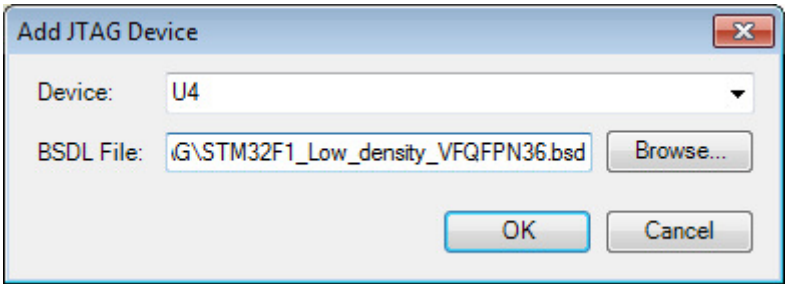


Figure 5 Associating a BSDL file to an IC in the schematic

The path to the BSDL file will be stored as a parameter of the device in the Altium project. Any plain text file format is acceptable for use as a BSDL file and the extension will automatically check that the file parses correctly. However the onus is on the user to ensure that the BSDL file is the correct one for the device chosen. An incorrect BSDL file may lead to incorrect and misleading results when using the **XJTAG Chain Checker** or **XJTAG Access Viewer**.

4.3.2. Defining JTAG Chain(s)

As outlined above, a TAP (Test Access Port) comprises a minimum of four signals: TDI (Test Data In); TDO (Test Data Out); TCLK (Test Clock), and TMS (Test Mode Select). An optional fifth signal, nTRST (Test Reset) may also be present, which disables boundary scan when held low.

It is essential that the JTAG chain (TAP) is routed to the correct pins on each JTAG-enabled device in the chain. For the chain to function correctly it must be possible to trace a route from the board TDI pin (where the chain enters the board), into TDI and out of TDO of each JTAG device in turn and then to the board TDO pin (where the chain leaves the board). It is possible to implement more than one chain on a single design, however each JTAG-enabled device may only be connected to a single JTAG chain. The **XJTAG DFT Assistant for Altium Designer** software extension provides a fully integrated way of ensuring scan chains are connected as intended and correctly.

In order to achieve this it is necessary to identify the TDI and TDO pins on each chain to determine how the PCB will be connected to the JTAG testing hardware. It is possible to define up to 4 scan chains in a single design. To select the TDI and TDO pins for each chain, click on the *Add* button next to the TDI and TDO list view, and this will open the *Add Chain* dialog box (*see Figure 6*).

The *Add Chain* dialog allows a name to be assigned to the chain and for the TDI and TDO pins to be selected from the pins on the board. Typically these pins will be test points or on a connector. To assign TDI either enter the device and pin designation directly in to the dialog box (for example, enter CN1.5 for Connector 1, Pin 5), or select a device and pin manually. If selecting manually, clicking the Select button will bring up the Select Device and Pin dialogue box showing all available devices. Selecting a device will

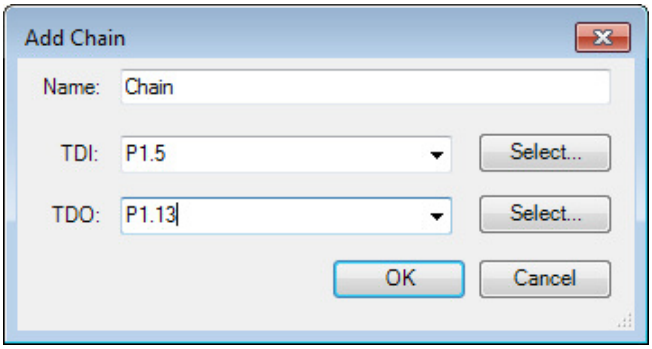


Figure 6: Adding a boundary scan chain

reveal all available pins on that device, with their net designations (if included). Select a pin and press OK. Repeat this process to assign TDO.
Note: Once TDI or TDO have been assigned the Select Device and Pin dialogue box will default to the same component. This can be overridden if necessary by deleting the Device name in the Filter box.Once TDI and TDO have been assigned and BSDL files have been added for all JTAG-enabled devices in the chain, the extension has enough information to automatically generate a JTAG chain route. The route is automatically generated each time the project is opened, therefore reflecting any changes made at the schematic level.

4.3.3. Categorising passive devices

There are two reasons for categorising passive devices on the board. Firstly, it is common for passive devices, such as resistors and links, to be used in the JTAG chain. These devices need to be categorised to allow the JTAG chain to be auto-routed successfully. Secondly, categorising series resistors will allow the **XJTAG Access Viewer** tool to provide a more accurate indication of the extent of JTAG access on the board.

Passive devices are categorised by assigning them a passive device descriptor (PDD) file, in a similar way to JTAG devices and BSDL files, except that PDD files do not need to be supplied externally. PDD files for common cases, such as a series resistor, pull resistor, series and pull resistor packs etc., are included with the **XJTAG DFT Assistant for Altium Designer** extension. More complex custom PDD files can be defined by the user through the extension's interface to cover any possible passive device configuration.

There are two methods for categorising passive devices. Devices can be manually searched for and categorised by clicking the *View uncategorised devices* button to open the *Uncategorised Devices* dialog (*see Figure 7*). Alternatively the **XJTAG DFT Assistant** can suggest categorisations automatically by clicking the *Suggest Categorisations* button. The *Suggest Categorisation* dialog will provide PDD files for any passive devices that can be auto-categorised (*see Figure 8*). To avoid categorising passive devices that will not affect the extent of JTAG access, the *Suggest Categorisation* dialog is limited to those devices already on nets with JTAG access.

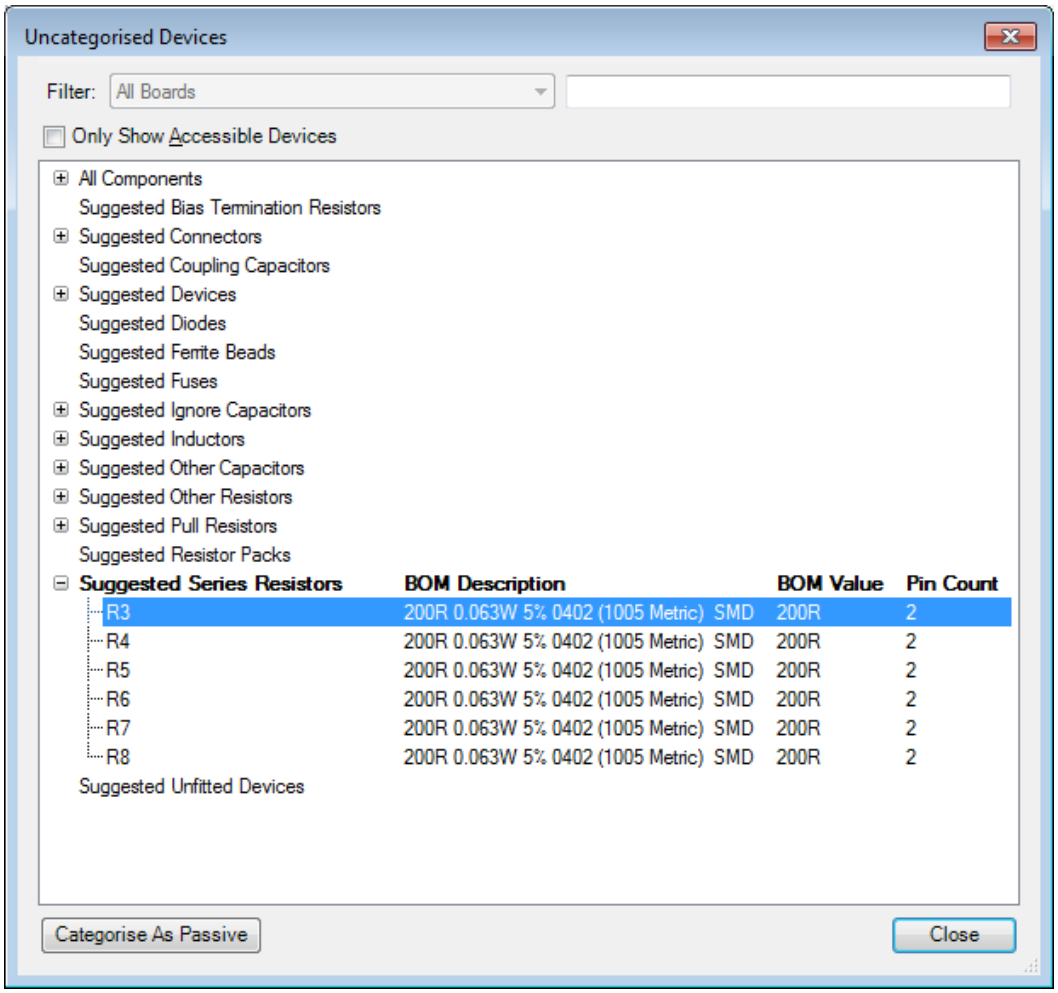


Figure 7: The Uncategorised Devices dialog box

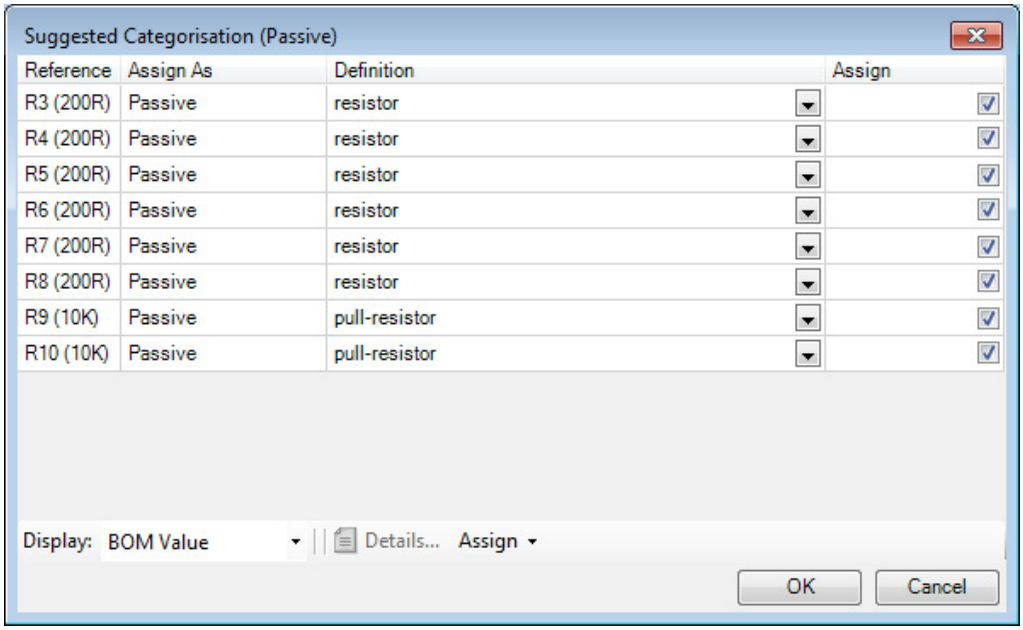


Figure 8: The Suggest Categorisation dialog box

To uncategorise an already categorised device, press the *View categorised devices* button which will bring up a list of all passive devices categorised so far. From here a device, or group of devices, can be selected and uncategorised.

4.3.4. Manually creating a passive device

To manually create a passive device (using a new PDD file) open the *Uncategorised Devices* dialog and select a device, either by navigating the tree view or typing the device reference into the filter box. Clicking the *Only Show Accessible Devices* checkbox will toggle between showing all devices in the circuit or only showing devices on nets with JTAG access. Once a device, or group of devices, is selected press the *Categorise As Passive* button to open the *Assign Device* dialog (*see Figure 9*).

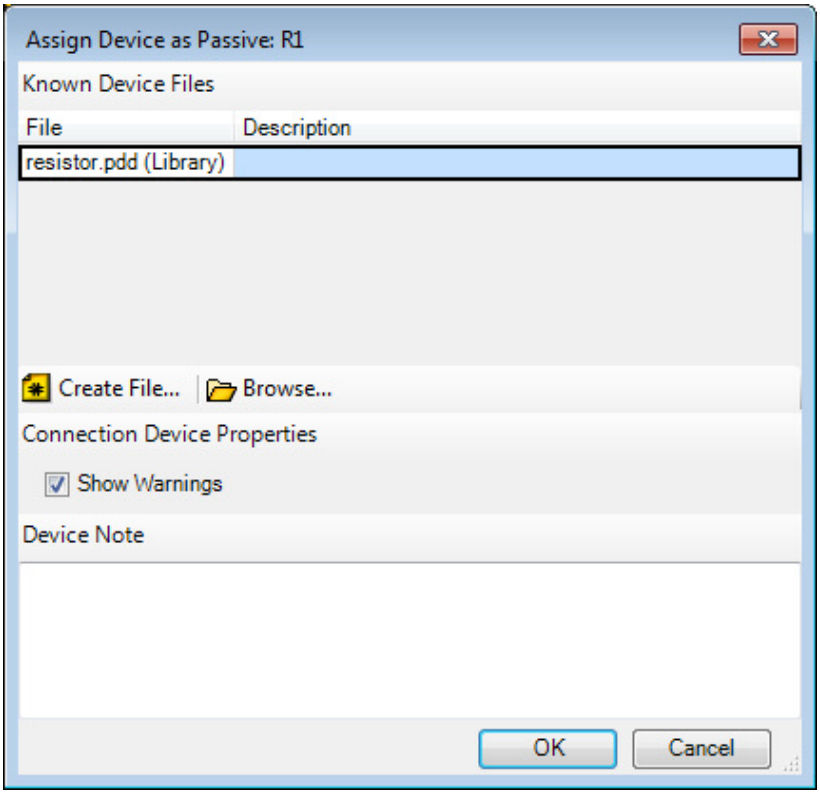


Figure 9: Assigning a device as a passive

The top half of the dialog will provide suggestions for possible PDD files that match the parameters of the device. Selecting one of these and pressing OK will categorise the device. If no suitable PDD file is present in the top list there are the options to browse for an existing PDD file that was created previously or to create a new one. Pressing the *Create File* button will open the New PDD File Dialog (*see Figure 10*).

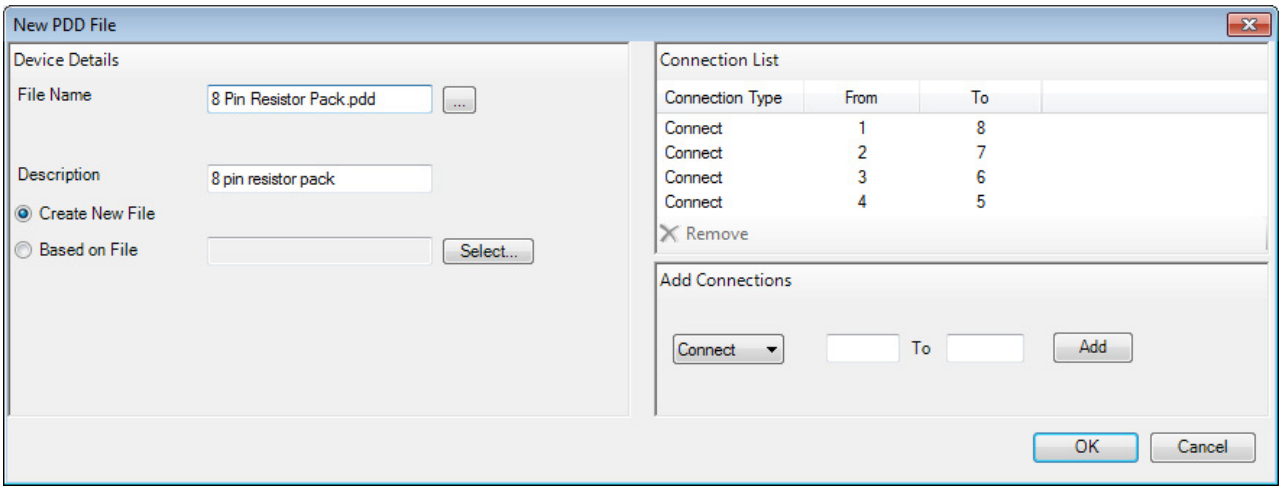


Figure 10: Creating a new PDD file

To create a new PDD file, enter a filename and (optionally) some description text and then add connections between pins. Connections can be of two types, either a simple connection (where the two pins are electrically linked or there is a low resistance value between them) or a pull connection (for pull resistors). Once a type is selected, and the pin numbers have been entered, press *Add* to add the connection to the list. Once all connections are added, click OK to create the new file.

Connections which do not fall into these types (e.g. terminations) should be left uncategorised – if the project is exported into **XJDeveloper** they can be set up there.

4.4. Check JTAG Chain

Once setup is complete, clicking on the *Check Chain* button will initialise the **XJTAG Chain Checker**. This will open the *Chain Check Results* dialog box (*see Figure 11*), giving a breakdown of any potential errors or causes for concern in the JTAG chains that have been defined.

The errors and warnings reported by the **XJTAG Chain Checker** are split into 3 categories; TAP net connection errors, TAP net termination errors and compliance pin errors. Connection errors are problems that prevent a JTAG chain being routed successfully and are classed as fatal errors as they will prevent any JTAG access through that chain. Termination errors are caused by TAP nets not being terminated to power or ground properly, potentially causing signal integrity issues. The errors and warnings will make recommendations for how best to prevent this. Compliance pins are pins on JTAG devices that must be set correctly to enable the device's boundary scan operation. The pins and values required are set out in the *Compliance Patterns* section of the BSDL file and the compliance pin errors will report any errors in the circuit design that prevent these pins being set correctly. If any errors or warnings are detected, the results can be optionally displayed in the *Messages* panel used by Altium Designer to display other board design issues.

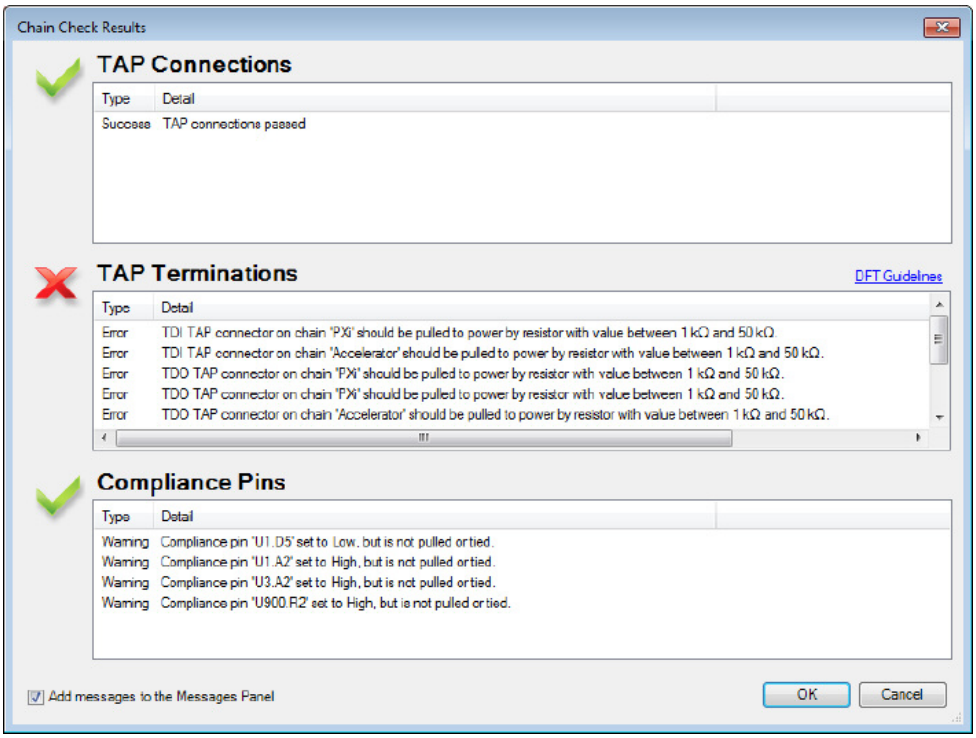


Figure 11: The Chain Check Results Dialog box

The full list of errors and warnings that are detected are shown below:

TAP net connection errors
- TAP net (TDI, TDO, TMS, TCLK or TRST) connected to the wrong pin(s) with respect to the associated BSDL file(s)
- TAP net connected to a power or ground net
- Two different TAP nets connected together
- Loop in a JTAG chain
- Two TDI pins connected to the same net
- Unable to route JTAG chain for some other reason

TAP net connection warnings
- All devices in chain do not share the same TMS or TCK

TAP net termination errors
- TDI, TDO or TMS not pulled to power
- TRST not pulled to ground
- No series resistor on TDO
- TCK not terminated to ground with a resistor and capacitor

TAP net termination warnings
- TDI, TDO or TMS pulled to power with a resistor of the wrong value
- TRST pulled to ground with a resistor of the wrong value
- TCK terminated with a resistor/capacitor of the wrong value

Compliance pin errors
- Compliance pin tied the wrong way
- Compliance pin pulled the wrong way with no other device on the net
- Compliance pin not connected

Compliance pin warnings
- Compliance pin not tied or pulled

Full list of faults detected by XJTAG DFT Assistant for Altium Designer

Note: The termination check and compliance pin check will not run if there are TAP net connection errors.

4.5. XJTAG Access Viewer

At any stage of the board setup, clicking on the *Show JTAG Access* button will highlight the JTAG access on each page of the schematic diagram. This feature shows the best level of access available on each net, as long as all JTAG devices categorised so far are connected up correctly. The nets will be colour-coded, as shown in *Figure 12*. The nets accessible to boundary scan testing will be highlighted using these colour codes, as shown in *Figure 13*.

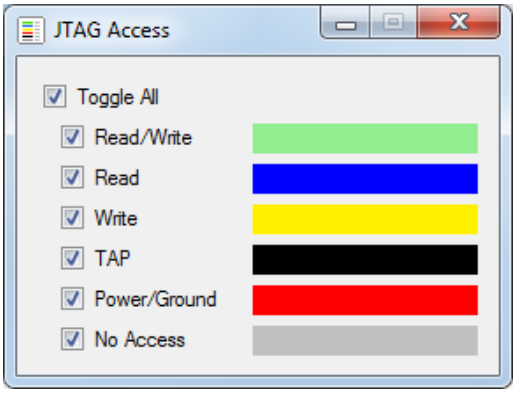


Figure 12: Colour-coded nets showing boundary scan access

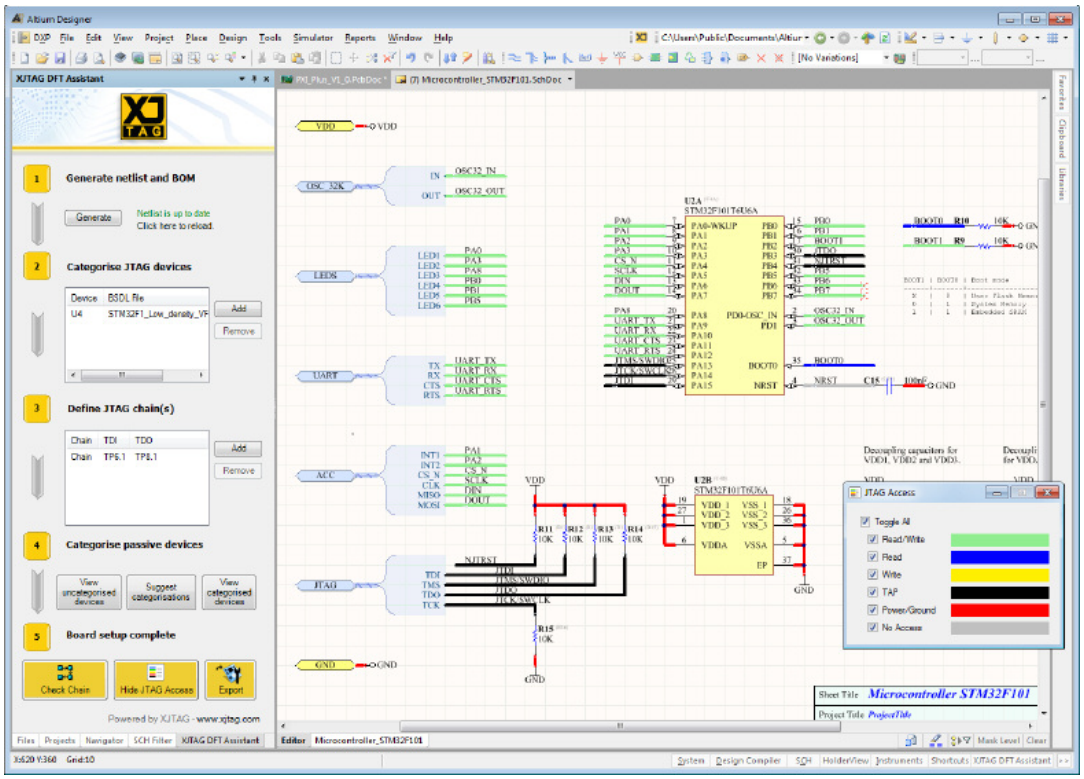


Figure 13: Screenshot showing colour-coded boundary scan access

Pressing the *Hide JTAG Access* button, changing project or closing Altium Designer will return all nets to their original colours.

5. Export XJDeveloper Project

At any stage, users with a licence from XJTAG can export the information they have entered as an **XJDeveloper** project. By clicking on *Export XJDeveloper Project*, the **XJTAG DFT Assistant for Altium Designer** will look for a valid **XJDeveloper** licence. If no licence is detected, the following box will appear (*Figure 14*):

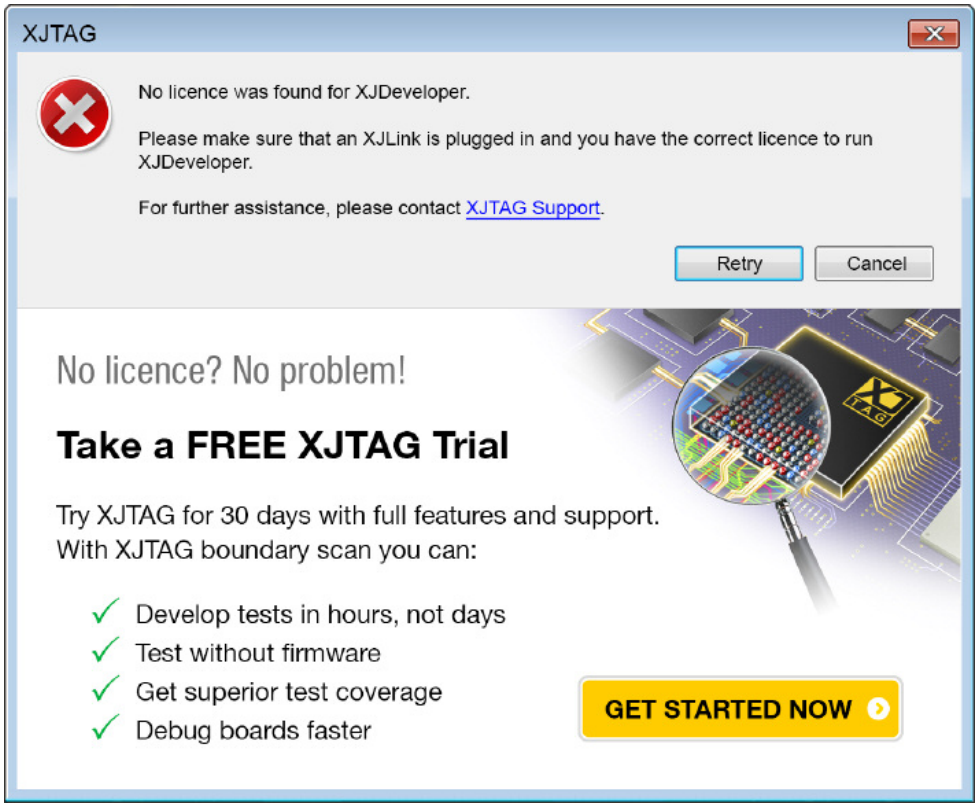


Figure 14: Missing XJDeveloper licence dialog box

If no valid **XJDeveloper** licence is available, click on *Get Started Now* to open a webpage detailing the free evaluation offer on XJTAG's website.

Please note, exporting requires V3.4 or higher of XJDeveloper

5.1. Boundary Scan test development

XJDeveloper is XJTAG's Integrated Development Environment (IDE) for the development and execution of interconnection and functional tests run over Boundary Scan. It provides all the functionality needed to execute boundary scan tests on a prototype board, as well as production tests in a manufacturing environment.

XJDeveloper includes an extensive library of functional tests for non JTAG-enabled devices. It also includes a powerful test development language called *XJEase*, which makes it easy to develop further tests and apply them through an *XJLink2 Controller*.

5.2. Migrating a project to XJDeveloper

The setup process completed within the **XJTAG DFT Assistant for Altium Designer** can be exported as an **XJDeveloper** project, and simply opened from within **XJDeveloper**. The user can then continue with the board setup process, by categorising the remaining non JTAG-enabled devices which have not been categorised in the *XJTAG DFT Assistant*. A full interconnectivity test can then be carried out on the PCB once manufactured, to identify a wide range of manufacturing faults. The full list of faults that can be detected using XJTAG's boundary scan technology is illustrated in *Figure 15*.

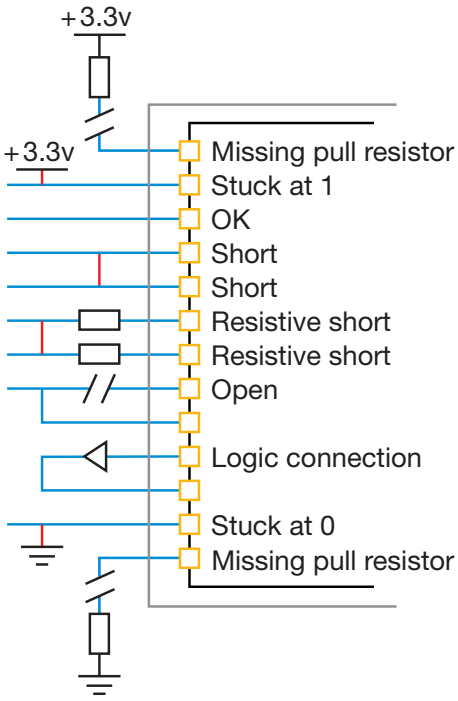


Figure 15: The full range of faults detectable using XJTAG's boundary scan technology

6. Troubleshooting

- **The XJTAG DFT Assistant extension does not appear on my Extensions page in Altium Designer**
  The extension requires Altium Designer 15 through version 24.7 and an active Altium subscription to download. The extension should then appear on the "Purchased" tab in the "Extensions and Updates" page in Altium Designer. If the extension still does not appear please contact your Altium support provider.

- **Error while generating netlist**
  There are a large variety of reasons why an error might occur at this stage.
  Please contact *support@xjtag.com* with details of the specific error you are seeing.
  If possible, a fix will be provided in a new release of the extension.

- **Registration reports "Unable to communicate with XJTAG server"**
  This error means the *XJTAG DFT Assistant* is unable to connect to the internet.
  An active internet connection is required in order to register for the *XJTAG DFT Assistant* extension.
  Once successfully registered, no further internet connection is required.

- **Chain Check – "Fatal Error: Cannot find a TDI pin or the final TDO pin connected to pin X.x."**
  This error means the chain check is unable to find a valid route for the JTAG chain. Please check that the TDI and TDO pins you have provided are correct. The most common cause of this error is an uncategorised passive device in the JTAG chain. The pin listed in the error is the last point in the JTAG chain reached before the auto-route failed, so this is a useful place to look for the issue.
  See *Section 4.3.3* for a guide on categorising passive devices.

- **Chain Check – Termination or Compliance errors are reported incorrectly**
  The chain check uses a variety of patterns to identify pull resistors on the schematic automatically. However this cannot always correctly identify all components. Specifically resistor references that do not begin with an R, or BOM values that contain other information apart from just a resistance, can cause problems. Results can always be improved by categorising any pull resistors or resistor packs on the TAP nets. See *Section 4.3.3* for a guide on categorising passive devices.
  Please contact *support@xjtag.com* if you are still having issues.

- **The JTAG Access colour scheme is stuck on**
  If Altium Designer crashes or otherwise closes unexpectedly while the JTAG Access colours are enabled they can become saved to the project. To return all nets to their normal colour simply right click a wire and select "Find Similar Objects…" in the context menu. Make sure the "Select Matching" checkbox is ticked and then OK the dialog. The line width and colour of all wire objects can then be edited at once.

- **Project files appear modified in source control systems after using the XJTAG DFT Assistant**
  The extension saves categorisations and net colour/width information to project files so they will show up as modified after the extension is used. If using a source control system please be aware of this, and if changes are discarded then categorisation information will be lost.

- **All categorisations are removed after moving the Altium project**
  BSDL files and PDD files used for categorisation are stored in a hidden folder called XJTAG inside the project directory. If this folder is not moved with the project then unfortunately all categorisations will be lost. Make sure to copy this folder with the project if you wish to keep your categorisation information.

Any other issues relating to the XJTAG DFT Assistant, or if you would like to submit a bug or feature request, please contact **support@xjtag.com**.

7. Further reading

For more information on XJTAG's boundary scan technology, visit **www.xjtag.com**.
For an extensive guide to Design For Test best-practices for boundary scan testing, visit **www.xjtag.com/about-jtag/design-for-test-guidelines**

About XJTAG

XJTAG is a world leading supplier of JTAG boundary-scan hardware and software tools. The company focuses on innovative product development and high quality technical support.

XJTAG products use IEEE Std.1149.x (JTAG boundary-scan) to enable engineers to debug, test and program electronic circuits quickly and easily. This can significantly shorten the electronic design, development and manufacturing processes.

XJTAG, based in Cambridge, UK, released version 1.0 of its boundary-scan tools in 2003 and starting from the UK, XJTAG has expanded and is now a business with multi-million dollar worldwide sales. XJTAG was the first boundary-scan solution to offer a common platform for use by design and development engineers, test engineers, contract manufacturers and field test engineers, providing testing of not only JTAG-enabled devices but non-JTAG devices as well. This change of emphasis towards test re-use and usability has driven the boundary-scan market forward, as board designers realised that they can have the test equipment on their benches and then re-use tests at production time.

XJTAG believes in being open – clients can see and edit the script files that are used to test for non-JTAG devices. If a revised device comes along, or the client has a problem, they can alter or debug the test themselves if they do not wish to (or are unable to) involve XJTAG.

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