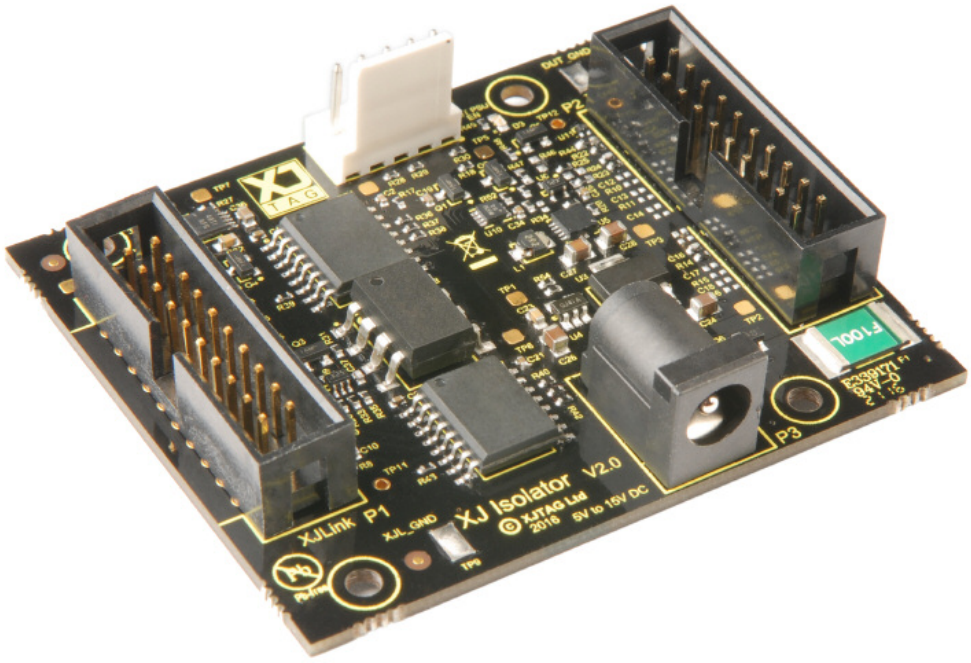
XJTAG®

XJIsolator Board

User Guide

Version 2.2



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1. Introduction

The XJIsolator provides galvanic isolation between a Device Under Test (DUT) and all other XJTAG hardware. Its design means the small board, which plugs directly into the DUT, can even be mounted inside a test fixture. It can also form part of a more extensive installation including other XJTAG test hardware, like the XJExtender board.

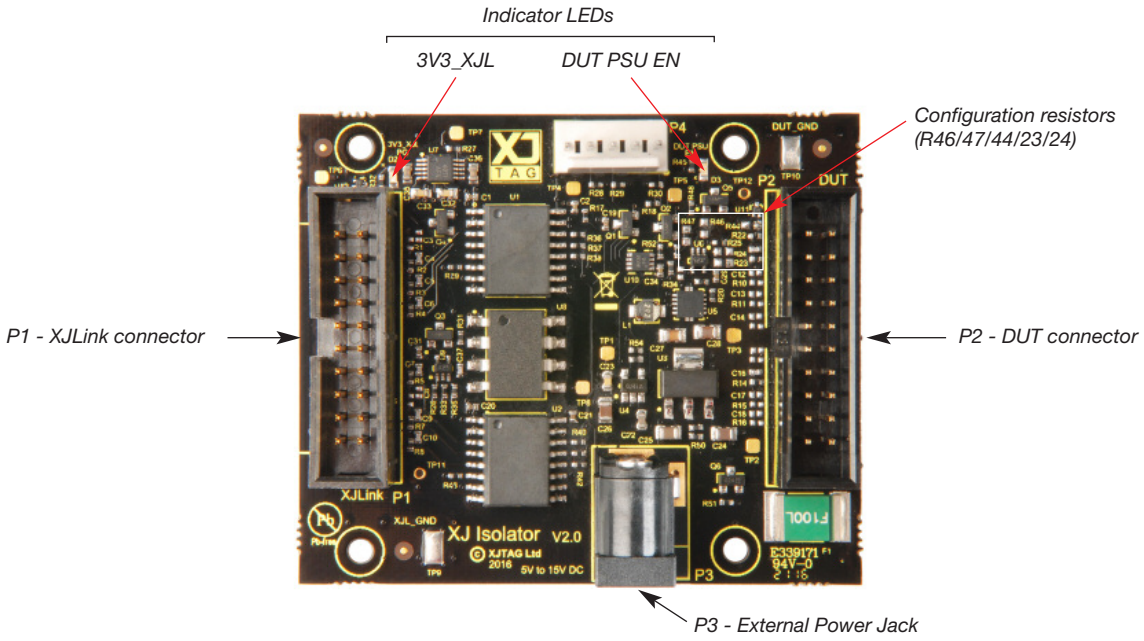


Figure 1 – XJIsolator position of connectors, configuration resistors and indicators

2. Features

- Working isolation voltages up to 443 Vrms
- Very low uni-directional propagation delay, typically 8 ns
- Connects directly to original XJLink or XJLink2
- Compatible with XJExtender and XJXDP
- Variable I/O voltage from 1.8 V to 3.3 V
- 5 V I/O voltage option available
- Offers 8 isolated signal channels configured as 6 downlink and 2 uplink
- Single power supply required, referenced to DUT ground
- Flexible power supply voltage: 5 V to 15 V
- LED indicators show power status
- Up to 50 MHz operation
- ESD protection
- Transparent to XJTAG software
- Can provide power to DUT

3. Specifications

Outer dimensions (including connectors)	64 mm length x 53.5 mm width x 14 mm height
Maximum TCK frequency	50 MHz
Maximum working isolation voltage (continuous operation)	443 Vrms
XJLink2 signaling and pin 1 power output voltage setting	1.8 V to 3.3 V
External power (P3)	5 V to 15 V (7 V to 15 V if using 5 V I/O option)
Maximum supply current	150 mA
Power supply plug	2.1 mm inner diameter, 5.5 mm outer diameter
XJLink2 & DUT connectors (P1 & P2)	20-pin, dual row, 2.54 mm pitch
Maximum DUT supply current (from pin 1 of P2)	100 mA

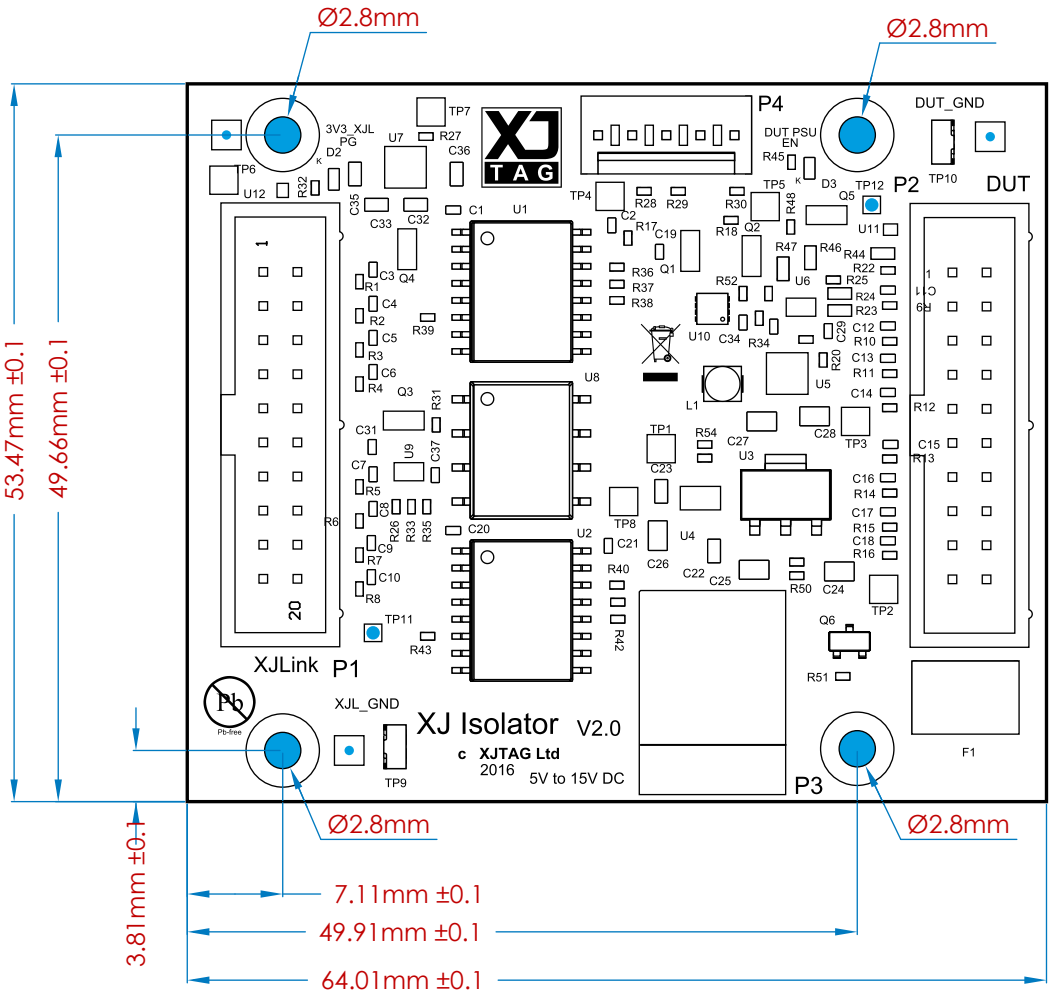


Figure 2 – Dimensions

4. Connector Pin Assignments

XJLink Connector P1

(20-way, 2.54 mm pitch)

DUT Connector P2

(20-way, 2.54 mm pitch)

Pin	Signal Name	I/O	Description		Pin	Signal Name	I/O	Description
1	VREF	IN	Reference voltage and power input		1	VADJ	IN/OUT	Default Configuration: Reference voltage out/DUT power
2	GND		Ground		2	GND		Ground
3	O1_XJL	OUT	Channel 1: Uplink (Output from P1)		3	I1_DUT	IN	Channel 1: Uplink (Input to P2)
4	GND		Ground		4	GND		Ground
5	I1_XJL	IN	Channel 2: Downlink (Input to P1)		5	O1_DUT	OUT	Channel 2: Downlink (Output from P2)
6	GND		Ground		6	GND		Ground
7	I2_XJL	IN	Channel 3: Downlink (Input to P1)		7	O2_DUT	OUT	Channel 3: Downlink (Output from P2)
8	GND		Ground		8	GND		Ground
9	I3_XJL	IN	Channel 4: Downlink (Input to P1)		9	O3_DUT	OUT	Channel 4: Downlink (Output from P2)
10	GND		Ground		10	GND		Ground
11	I4_XJL	IN	Channel 5: Downlink (Input to P1)		11	O4_DUT	OUT	Channel 5: Downlink (Output from P2)
12	GND		Ground		12	GND		Ground
13	O2_XJL	OUT	Channel 6: Uplink (Output from P1)		13	I2_DUT	IN	Channel 6: Uplink (Input to P2)
14	GND		Ground		14	GND		Ground
15	I5_XJL	IN	Channel 7: Downlink (Input to P1)		15	O5_DUT	OUT	Channel 7: Downlink (Output from P2)
16	GND		Ground		16	GND		Ground
17	I6_XJL	IN	Channel 8: Downlink (Input to P1)		17	O6_DUT	OUT	Channel 8: Downlink (Output from P2)
18	GND		Ground		18	GND		Ground
19	NO_CONNECT		No connect		19	NO_CONNECT		No connect
20	GND		Ground		20	GND		Ground

Isolation Barrier

5. Configuration

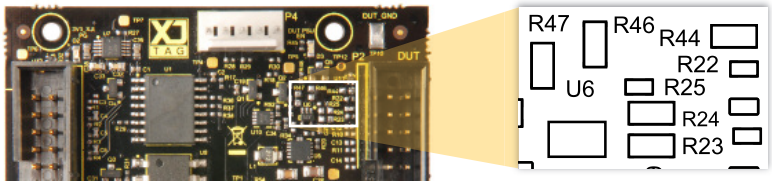
The channel assignment in XJIsolator boards is fixed: channels 1 & 6 are uplink (communication from DUT to XJLink2) and the remaining 6 channels are downlink (communication from XJLink2 to DUT). A single channel would be used to transmit one JTAG signal. For example one of the uplink channels would be used for TDO and three of the downlink channels would be used for TDI, TMS, and TCK on a standard JTAG connection.

The XJIsolator board supports I/O voltage from 1.8 V to 3.3 V. To support 5 V I/O, two resistors should be changed as shown in the following table (note XJLink2 bank voltage should be set to 3.3 V when the XJIsolator board is configured for 5 V I/O and the power supply should be a minimum of 7 V).

Component	Package size	V_{IO} range 1.8 V to 3.3 V (default)	Extended V_{IO} range to 5 V
R46	0603	NF	20 kΩ (1%)
R47	0603	0 Ω	10 kΩ (1%)

By default the voltage reference for the I/O signals on P2 is provided by the XJLink. Alternatively, the XJIsolator board can be configured to use a voltage supplied from the DUT on Pin 1 of P2 as the reference voltage. To switch between these modes two resistors need to be changed, as shown in the following table.

Component	Package size	XJLink provides I/O reference voltage (default)	DUT provides I/O reference voltage on P2.1
R23	0603	0 Ω	NF
R24	0603	NF	0 Ω



When using the DUT to set the I/O voltage, the power output on pin 1 of the XJLink should still be enabled.

The XJIsolator can also be configured to provide up to 100 mA to power the DUT. If this is required then the power is provided on pin 1 of P2; the I/O reference select resistors must be in their default states, as shown in the table above, and the resistor R44 requires fitting as shown in the following table.

Component	Package size	Power not provided on P2.1 (default)	Power is provided to the DUT on P2.1
R44	0603	NF	0 Ω

If the DUT does not require a reference voltage pin 1 on P2 can be left disconnected from the UUT.

6. Operating Instructions

Quick start instructions

1 Connect the XJIsolator XJLink port (P1) to the XJLink2 using 20-way ribbon cable
2 Connect the XJIsolator DUT port (P2) to the DUT using 20-way ribbon cable
3 Set XJLink bank voltages to match DUT I/O voltage
4 Provide power to P3 (5 V to 15 V)
5 To enable the XJIsolator, enable power on XJLink2 pin1 (select Bank 1 ‘Power On’ on Pin Mapping screen)
6 3V3_XJL PG LED is illuminated when XJLink2 pin1 is powered
7 DUT PSU EN LED is illuminated when outputs are enabled and reference voltage is available on pin 1 of P2

Detailed description

The XJIsolator connects to the XJLink2 and DUT via standard 20-way 0.1” ribbon cables. For the highest clock speeds, the ribbon cables should be kept as short as possible.

The DUT part of the XJIsolator board needs to be provided with external power, via connector P3, at any voltage between 5 V and 15 V. The power supply should be able to supply up to 100 mA and the ground terminal of the power supply should be at the same potential as DUT ground. Connector P2 can provide up to 100 mA on pin 1 to power the DUT or alternatively this pin can be used as a reference voltage for the DUT. The XJLink side of the XJIsolator board draws little current and is powered directly from the XJLink2.

Configure the Pin Mapping to match the direction of each channel. The output voltage and input voltage threshold should match the DUT and be the same for both banks. Pin 1 should be set to “Power On”. All configurable even pins should be set as Soft GND.

Figure 3 shows an example Pin Map for two chains. The I/O pins on P2 are high impedance until power is provided to pin 1 of P1 by the XJLink2. At this point the I/O pins on P2 (DUT connector) become active and pin 1 on P2 is powered at the XJLink output voltage level. A number of voltage regulators are included on the board including a switch mode regulator operating at a nominal frequency of 3 MHz.

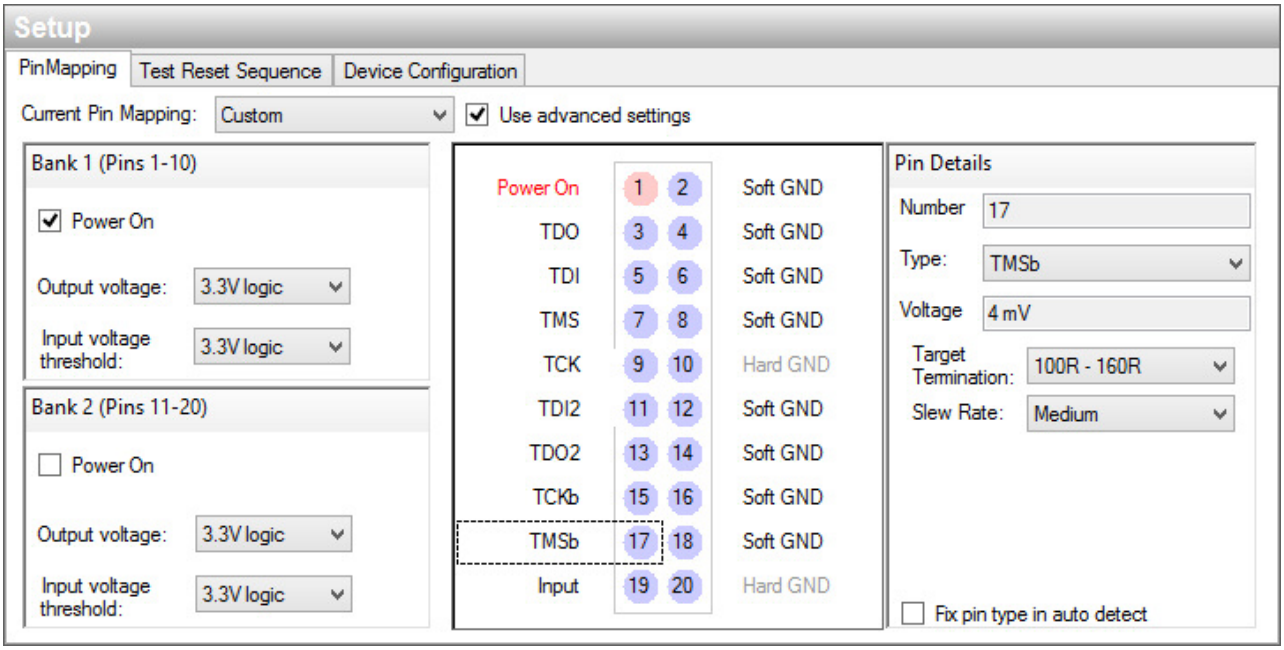


Figure 3 – Example Pin Map for default configuration

Use of the XJIsolator system is transparent to the XJTAG software. Tests can be developed with the board connected directly to the DUT and then an XJIsolator board added at a later date when the test system is deployed. As long as the pin map is suitable for the XJIsolator board, no software changes are required.