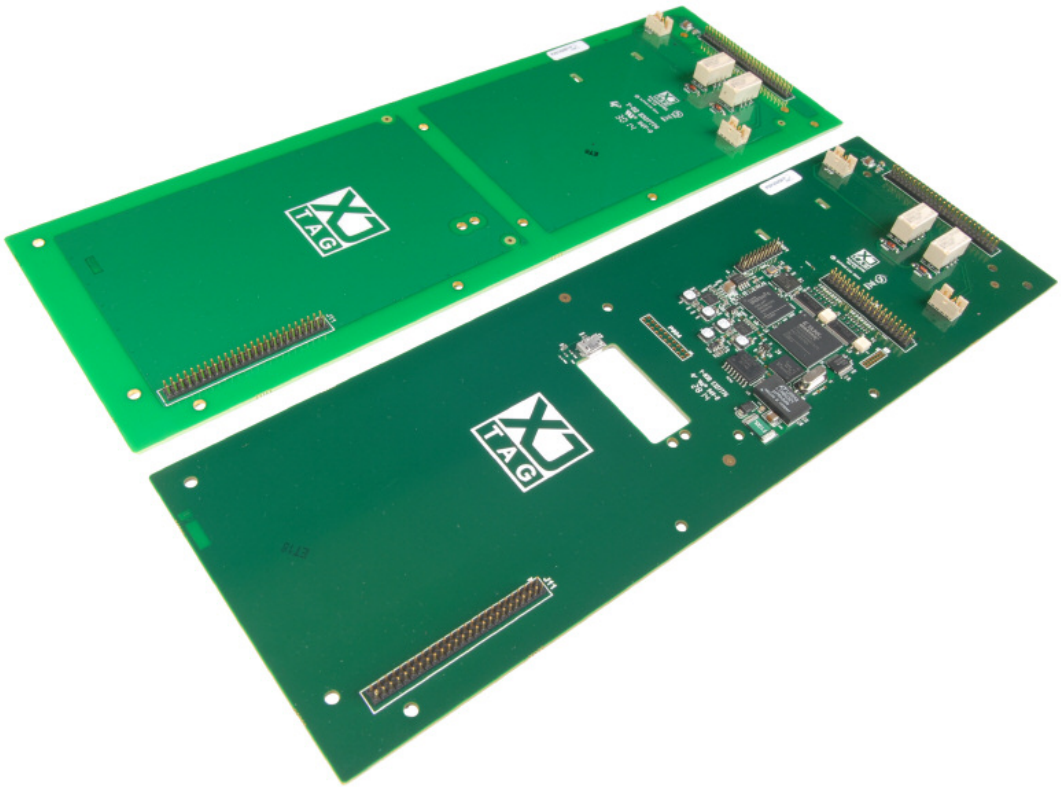
XJTAG®

XJLink2-CFM Hardware

User Guide

Version 1



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1. Introduction

The XJLink2-CFM is an application module compatible with the Teradyne Multi-Function Application Board (MFAB). It brings XJTAG's boundary scan test and programming tools to a Teradyne TestStation™.

One XJLink2-CFM can provide up to four independent JTAG TAPs when used in conjunction with extender boards that distribute the signals to the MFAB's different slots.

To test multiple PCBAs simultaneously, additional XJLink2-CFM boards can be fitted into spare slots on the MFAB.

This guide describes the XJLink2-CFM and how to connect it plus any extender boards to the MFAB.

2. Description of the XJLink2-CFM

The XJLink2-CFM has 18 interface pins that can be independently configured in software to provide different functions.

It has the following capabilities:

- Provides up to four independent JTAG TAPs.
- Each of the 18 interface pins can be configured to be a programmable I/O.
- The 18 interface pins are grouped into two independent banks.
  Each bank's operating voltages can be configured in software or set by an externally applied voltage.
- Digital outputs have selectable drive strength and slew rate.
- I/O pins provide programming capability over JTAG, I2C, SPI, SWD, and custom protocols.
- Accelerated programming. The XJLink2-CFM's advanced features achieve programming speeds close to the theoretical maximum of the target device.

Figure 1 shows the XJLink2-CFM's main connectors. The 18 configurable signals are present on J8, from where a ribbon cable is used to distribute them to connectors J9 and J10 on the CFM and on any expander boards.

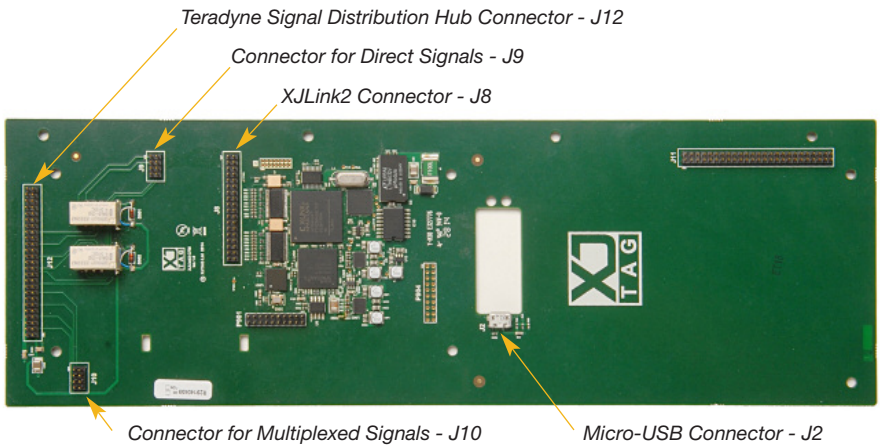

Figure 1 – XJLink2-CFM Connectors

The XJLink2-CFM connects to the MFAB via connector J12.

A PC running XJTAG software needs to be connected to the XJLink2-CFM's micro-USB socket, J2.

Table 1 shows the options available for each of the 18 software-configurable pins on connector J8. If required, frequency and voltage measurements can also be performed on any I/O pin.

	XJLink Pin[1]	J8 pin	JTAG	PIO	Path Select[2]	VREF[3]	Soft GND[4]	Configurable I/O voltages	Configurable Terminations
Bank 1	1	1	✓	✓		✓		✓	✓
	2	3	✓	✓		✓	✓	✓	✓
	3	5	✓	✓		✓		✓	✓
	4	7	✓	✓		✓	✓	✓	✓
	5	9	✓	✓		✓		✓	✓
	6	11	✓	✓		✓	✓	✓	✓
	7	13	✓	✓		✓		✓	✓
	8	15	✓	✓		✓	✓	✓	✓
	9	17	✓	✓		✓		✓	✓
Bank 2	11	21	✓	✓	✓	✓		✓	✓
	12	23	✓	✓		✓	✓	✓	✓
	13	25	✓	✓		✓		✓	✓
	14	27	✓	✓		✓	✓	✓	✓
	15	29	✓	✓		✓		✓	✓
	16	31	✓	✓		✓	✓	✓	✓
	17	33	✓	✓		✓		✓	✓
	18	35	✓	✓		✓	✓	✓	✓
	19	19	✓	✓		✓		✓	✓

Table 1 – Options for Software-Configurable Pins on J8

[1] The XJLink pin is the pin shown in the software when the pinout is configured.
[2] Configuring this XJLink2 pin as Power Out routes signals through the accelerator FPGA to enable accelerated or concurrent programming.
[3] Vref input takes an external voltage (e.g. from the DUT) and uses it to set the bank voltage. Each bank can have its own Vref source.
[4] Soft Grounds provide a low-impedance connection to ground that can be used in the construction of twisted pairs to reduce crosstalk.

Note: Although pin 1 of the XJLink2 can supply power, it only has low current capability and should not be used to power external circuitry.

3. Routing the Signals

Each slot of the MFAB has only four direct signals and four multiplexed signals available. To use all of the CFM's eighteen signals, it is therefore necessary to use additional slots and to connect to them with a ribbon cable.

It is best practice to route the four JTAG signals to direct signal pins and not to split them between different slots. If a Test Reset signal is needed, it is normally routed on one of the multiplexed signals on the same slot.

As shown in Table 1, connector J8 has 18 software-configurable pins. Signals to/from those pins are distributed around this board and any expander boards using a multi-section ribbon cable that connects to J9 and J10 on each board as shown in Figure 2 and Figure 3.

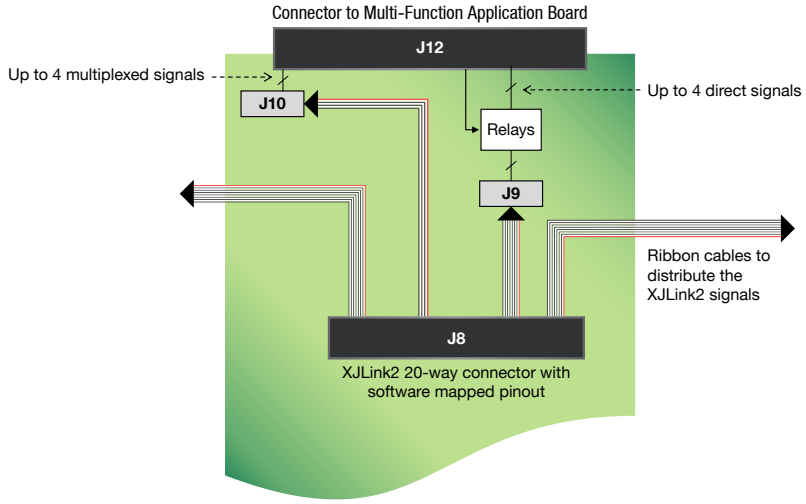

Figure 2 – Ribbon Cable Routing for the XJLink2 Signals

Each CFM and expander board routes signals between its J10 connector and the MFAB's multiplexed signal pins; its J9 connector interfaces to the MFAB's direct signal pins via relays.

Figure 3 and Figure 4 show a setup using one XJLink2-CFM with three expander boards to utilise all of its 18 signals. Sixteen of the configurable signals are routed to direct signal pins and the remaining 2 are routed to the multiplexed signal pins of slot 2.

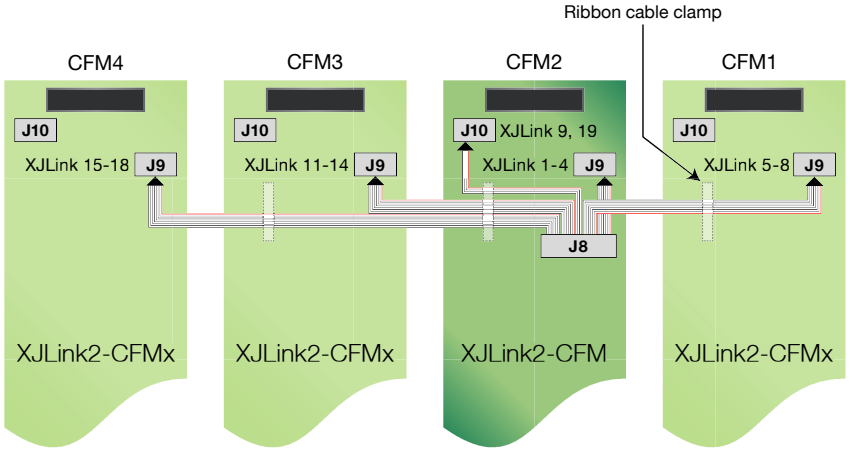

Figure 3 – Recommended Ribbon Cable Routing When Using all 18 Signals

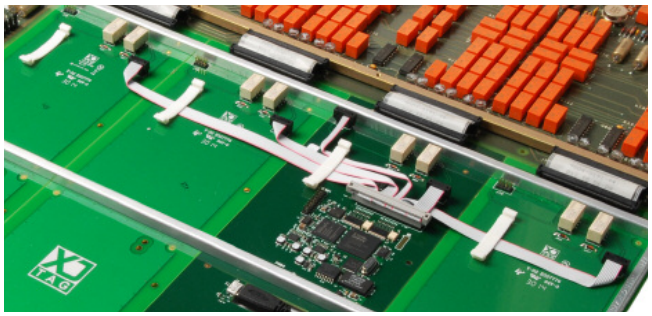

Figure 4 – Distributing the XJLink2 Signals

The connections that the PCB makes between J9/J10 and the MFAB interface on J12 are described in Table 2.

J12 Pin	Signal	Function
3	MUX4	Signal to/from J10 pin 7
7	MUX3	Signal to/from J10 pin 5
11	MUX2	Signal to/from J10 pin 3
15	MUX1	Signal to/from J10 pin 1
20	RELAY1	Input from the Teradyne system that controls a relay to isolate the DIR signals from the testbed. 0 V connects J9 pins 7 & 5 to this connector
23	DIR4	Signal to/from J9 pin 7 when RELAY1 is at 0 V. Otherwise: open-circuit
24	RELAY2	Input from the Teradyne system that controls a relay to isolate the DIR signals from the testbed. 0 V connects J9 pins 3 & 1 to this connector
27	DIR3	Signal to/from J9 pin 5 when RELAY1 is at 0 V. Otherwise: open-circuit
31	DIR2	Signal to/from J9 pin 3 when RELAY2 is at 0 V. Otherwise: open-circuit
35	DIR3	Signal to/from J9 pin 1 when RELAY2 is at 0 V. Otherwise: open-circuit
8, 10, 12, 14	Power In	Fused on-board at 1 A
1, 2, 4, 6	FP5V	Power in for on-board relays
5, 9, 13, 17, 21, 25, 29, 33, 37, 39, 43, 45	GND	
16, 18, 19, 22, 28, 30, 32, 34, 36, 38, 40, 41, 42, 47, 48, 49, 50	nc	Not connected

Table 2 – XJLink2-CFM J12 Main Connector Pinout

4. Recommended Signal Routing

Table 3 shows a recommended signal routing when using all 18 signals. In this example, one XJLink2-CFM is used with three extender boards and a multi-section ribbon cable that has 6 connectors. Sixteen of the XJLink2-CFM's signals are routed to the direct pins on the Teradyne MFAB, and the remaining two signals are connected to multiplexed pins. The XJLink2-CFM is placed in slot 2, with extender boards in the remaining three positions.

Ribbon Cable Section	J8 pin	XJLink Pin[1]	Ribbon connection	CFM slot	CFM pin	Fixture Receiver Interface Pin
1	1	1	J9 pin 1	2	DIR1	B28
	3	2	J9 pin 3	2	DIR2	A29
	5	3	J9 pin 5	2	DIR3	B34
	7	4	J9 pin 7	2	DIR4	A35
2	9	5	J9 pin 1	1	DIR1	B8
	11	6	J9 pin 3	1	DIR2	A9
	13	7	J9 pin 5	1	DIR3	B14
	15	8	J9 pin 7	1	DIR4	A15
3	17	9	J10 pin 1	2	MUX1	B4
	19	19	J10 pin 3	2	MUX2	A19
4	21	11	J9 pin 1	3	DIR1	B48
	23	12	J9 pin 3	3	DIR2	A49
	25	13	J9 pin 5	3	DIR3	B54
	27	14	J9 pin 7	3	DIR4	A55
5	29	15	J9 pin 1	4	DIR1	B68
	31	16	J9 pin 3	4	DIR2	A69
	33	17	J9 pin 5	4	DIR3	B74
	35	18	J9 pin 7	4	DIR4	A75

Table 3 – Recommended Signal Routing When Using all 18 Signals

[1] The XJLink pin is the pin shown in the software when the pinout is configured.

5. Powering the Board

The XJLink2-CFM is powered from the Teradyne MFAB connector J12 using pins 8, 10, 12, and 14.

Input voltage	7 – 18 V, nominal 12 V
Current	500 mA max.

6. Configuring XJLink2-CFM Interface Voltages

The 18 interface pins on the XJLink2-CFM are divided into two banks of nine. Each bank can operate at a different voltage level.

Bank 1	XJLink pins 1 – 9
Bank 2	XJLink pins 11 – 19

Setting the Bank Voltages

The voltage domain used for each bank can be set in software, either by selecting a standard logic level or by defining a custom voltage in the Advanced Settings. The input and output voltage levels can be set independently.

Output voltage range	1.1 V to 3.5 V in 0.1 V steps
Output voltage tolerance	±5%, typically ±3%

As an alternative to setting the bank voltages in software, the bank voltage can be made to mirror an external value. This is done by configuring a pin in software to have type VREF, VREF1, or VREF2 and applying a voltage to that pin. The bank voltage will then be set to match the applied voltage. Each bank can have its own Vref source. For details of how to use a common reference voltage source for both banks or two individual ones, refer to the Help System's XJLink2 section.

Interface Logic Voltage Characteristics

By default, the logic levels on the interface will be determined by the selected bank voltage. If standard logic levels are chosen, the voltage characteristics will be as shown in Table 4.

Bank Voltage	VIL max	VIH min	VOL max	VOL min	Load conditions
3.3	0.8	2	0.4	2.4	100 Ω
2.5	0.7	1.7	0.4	2	100 Ω
1.8	0.4	0.9	0.4	1.35	100 Ω
1.5	0.4	0.85	0.4	1	100 Ω
1.2	0.4	0.75	0.4	0.8	133 Ω

Table 4 – Interface Logic Voltage Characteristics

If a custom level is defined for the logic voltages, or the bank voltages are set using a Vref input, the user should refer to the XJTAG Help system for details of the logic thresholds that will apply.

Configuring Output Pin Characteristics

The drive strength and slew rate of any pin being used as an output from the XJLink2-CFM can be configured to maintain high speed, high quality signals.

Slew rate – each output pin can be given one of three slew rates to control the signal's rise and fall times. The value can be set to fast, medium, or slow on a pin-by-pin basis.

Drive strength – a drive strength can be set independently for each output pin. It is defined in terms of the series termination impedance of the net being driven.

7. Cable Restraints

The XJLink2-CFM and extender boards have holes for cable restraints as shown in Figure 5. These allow a cable-tie to secure the USB cable, and the supplied clamp to hold the ribbon cable in place.

Suitable replacement ribbon cable clamp: Richco snap-in nylon flat cable clamp, FCCS-2.

In addition, each board provides an electrically isolated connector (J11) that can be used as an anchor point for a Teradyne system ribbon cable.

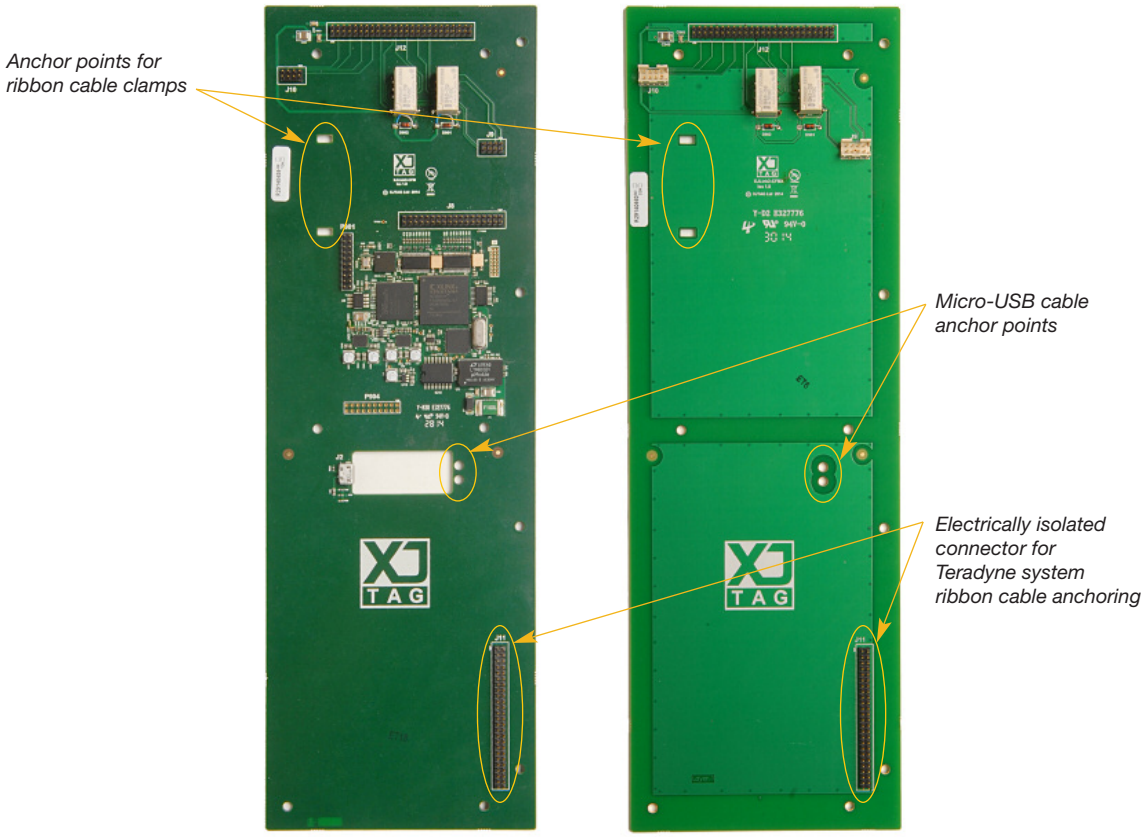

Figure 5 – Location of Mechanical Cable Anchor Points

8. Specification

USB Interface	USB 2.0 (480 Mbps), compatible with USB 1.1 The board is not powered over USB (voltage sense only)	
JTAG Signals	TCK	10 kHz to 166 MHz in steps of 0.05 MHz
Frequency Measurements	The frequency of a signal on any general-purpose pin can be measured	
	Input range	1 Hz – 200 MHz
	Accuracy	±10 ppm
	Selectable measurement period	1 ms, 10 ms, 100 ms, 1 s, 10 s
Voltage Measurements	The voltage on any general-purpose pin can be measured	
	Input range	0 – 5 V
	Accuracy	± (0.2% + 10 mV) at 15 – 35 °C
	Input impedance	>900 Ω